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Fabrication and Transport Properties of Gate-All-Around Silicon Quantum Wire Transistor

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A novel fabrication method of silicon quantum wire Gate-All-Around Transistor (GAAT), in which the gate oxide and the gate electrode are wrapped around the ultra fine silicon quantum wire, has been proposed. In order to verify one-dimensional (1D) subbands effects, we have studied quantum transport in Si quantum wire GAAT with a width of 50nm at low temperatures in zero-magnetic field and in fields up to 10T. Electrical population of 1D subbands and magnetic depopulation of 1D subbands are clearly observed.

1. Introduction

Silicon metal-oxide-semiconductor field-effect transistors (Si MOSFETs) are an excellent model system for physics experiments on many aspects of two-dimensional electron gas (2D EG). When the transverse dimensions of an ideally uniform electron channel are comparable to the electron wavelength, such a MOSFET can be transformed into an experimental device for studying the transport of electron confined to 1D channel. Recent advances in microfabrication have made possible the study of extremely narrow channel devices. Many lateral confinement schemes have been tried to achieve 1D channel. In the past few years, in contrast to electrostatic confinement using narrow gate, several attempts[1],[2],[3] have been made to realize physical confinement in Si nanostructures using the Si / SiO_2 high potential barrier, which would give greater electron confinement. In this work, employing anisotropic wet chemical etching and thermal oxidation, we have fabricated Si quantum wire GAAT, in which the gate oxide and the gate electrode are wrapped around the ultra-fine Si quantum wire between source and drain. In addition, the electrical- and magneto-transport properties of Si quantum wire GAAT are examined to observe 1D subband effects.

2. Device Fabrication

The fabrication process of Si quantum wire GAAT is schematically shown in Fig.1. The starting substrates are 10-15 Ωcm p-type (001)-oriented SIMOX (Separation by IMplanted OXygen) wafers. In the first step, SiO_2 mask patterns are fabricated on an active Si island. (Fig.1(a)). Next anisotropic wet etching is performed with the EPW[4] (E:ethylendiamine, P:pyrocatechol, W:water) etchant to form the Si wire with a trapezoidal cross-sectional profile. (Fig.1(b)) Then SiO_2 mask and the buried oxide layer underneath the Si wire are removed simultaneously by a buffered HF so that the free-standing Si wire is formed. This

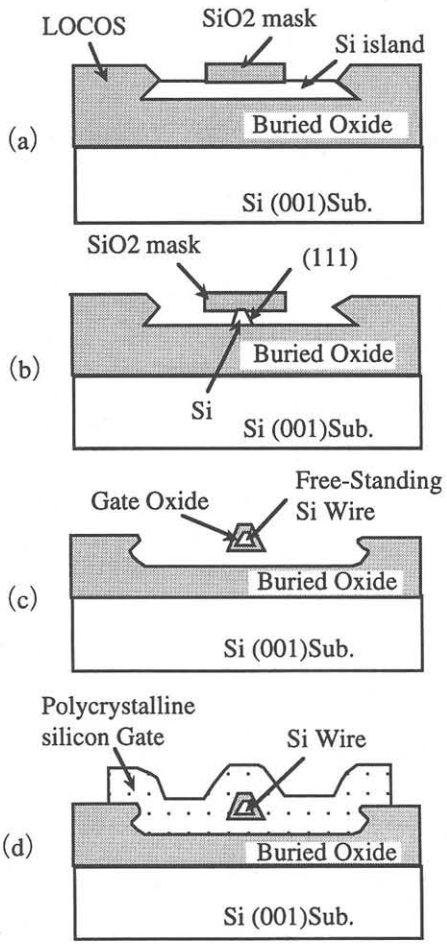

Fig. 1 Fabrication process of device used in this study.
(a) LOCOS isolation and SiO2 mask patterning.
(b) Anisotropic wet chemical etching.
(c) Removing SiO2 mask and thermal oxidation.
(d) Polycrystalline silicon gate formation.

wire is supported by its extremities which will later on become n+ source / drain region. The wire is left undoped in order to avoid quantum level broadening from elastic scattering. Next a thermal oxidation is performed to form gate oxide and make the free-standing Si wire narrower. (Fig.1(c)) Finally, polycrystalline silicon gate electrode is deposited in an LPCVD reactor and patterned. (Fig.1(d))
Figure 2 is the cross-sectional transmission electron microscopy (XTEM) image of Si quantum wire GAAT. (Note that this XTEM image is obtained after all measurements discussed below.) Using this new fabrication method, the 50nm wide Si quantum wire with triangular cross-sectional profile, which is fully embedded in SiO_2 has been successfully formed. The width variation along the wire is also confirmed to be within 10% by a scanning electron microscopy examination.

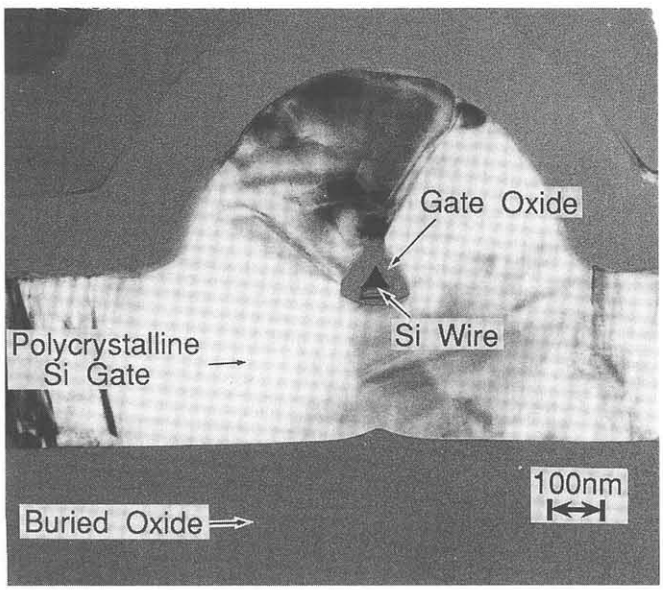

Fig. 2 XTEM image of the Si quantumwire GAAT with a width of 50nm.

3. Results and Discussion

The conductance measurements are performed by a conventional low-frequency lock-in technique at 1.5K. Fig. 3 shows the conductance of Si quantum wire GAAT with a width of 50nm as a function of gate voltage. Clear step like conductance oscillations are observed, which we believe is the direct reflection of the 1D subband effect. These oscillations persist up to ~40K, and 20mV of Vsd. Similar features are also observed on a separate device on the same wafer. To discuss these data quantitatively, we roughly estimate the lowest subband separation ΔE_{theory} of the 50nm wide wire. Using a square well approximation for simplicity, ΔE_{theory} is given by

$$\Delta E_{theory} = \frac{3\pi^2\hbar^2}{2m^*W^2} \qquad (1)$$

where W is the width of the wire (=50nm), and m* is the effective electron mass (=0.19m_0). This theoretical value ΔE_{theory}~2.4meV can be compared with an energy spacing $\Delta E_{exp.}$ of the oscillations estimated from the gate voltage spacing ΔVg. With approximation of the inversion layer as a narrow 2D EG, $\Delta E_{exp.}$ is given by

$$\Delta E_{exp.} = \frac{C \cdot \Delta Vg \cdot \pi\hbar^2}{2m^*e} \qquad (2)$$

where C is the capacitance between the gate electrode and the wire. With this equation (2), a capacitance C of 1.08E-7 F/cm^2 (from 32nm gate oxide on the (001) surface) and ΔVg ~0.7V shown in Fig.3 gives an energy spacing $\Delta E_{exp.}$ of ~3meV. This experimental energy spacing $\Delta E_{exp.}$ is consistent with the theoretical value ΔE_{theory}~2.4meV.

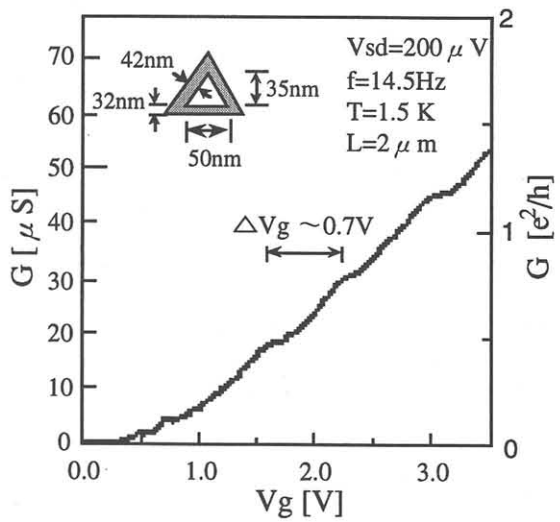

Fig. 3 Conductance of Si quantum wire GAAT with a width of 50nm as a function of gate voltage at 1.5K.

Figure 4 shows a magneto-conductance of 20 paralell wires GAAT with a width of 50nm. The magnetic field is perpendicular to the (001) surface. The data for magnetic filed applied parallel to the (001) surface show no oscillation, which indicates the observed oscillations are identified as quantum oscillations related to the Shubnikov-de Haas (SdH) effect in narrow electron channel on the (001) surface. Fig. 5 shows an experimental subband index number n-versus-(1/B) plot deduced from SdH oscillations shown in Fig.4. It can be seen that, similar to results reported before[5],[6], the dependence of n on 1/B departs from lineality at higher 1/B values. This behavior is characteristic of magnetic depopulation of 1D subbands[7]. The deviations from lineality in n-versus-(1/B) plot appear

because the cycrotron-orbit diameter d_c becomes larger than the Si quantum wire width[8]. This diameter d_c is given by

$$dc = 2\left[\frac{\hbar(2n+1)}{eB}\right]^{1/2} \quad (3)$$

According to Fig.5, the deviation from lineality sets in between B^{-1}~$0.13T^{-1}$ at n=2 and B^{-1}~$0.17T^{-1}$ at n=3. Conseqently, we obtain d_c=41nm<W<56nm, which nicely brakets our actual wire width , W=50nm.

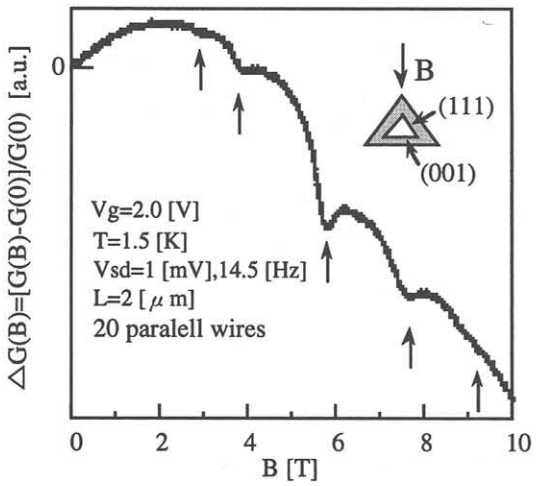

Fig. 4 Magneto-conductance of 20 paralell wires GAAT with a width of 50nm at 1.5K, applying magnetic field perpendicular to the (001) surface.

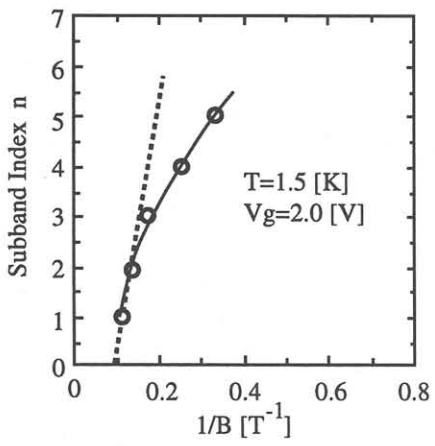

Fig. 5 Plot of subband index number n vs 1/B deduced from SdH oscillation shown in Fig. 4.

4. Conclusion

We conclude that the proposed fabrication method realizes Si quantum wire GAAT, in which the gate oxide and the gate electrode are wrapped around the ultra fine (~50nm) Si quantum wire. Conductance measurements of the device display a clear oscillatory behavior as a function of gate voltage. Assuming 1D subband effect, the experimental value is consistent with the theoretical estimates. In addition, we have observed magnetic depopulation effect of 1D subbands.

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