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Extremely Large Amplitude of Random Telegraph Signals in a Very Narrow Split-Gate MOSFET at Low Temperatures

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We have observed very large amplitude (≈90%) of Random Telegraph Signal (RTS) near the pinch off voltage at very low temperature (1.5K) in a very narrow, short channel n-MOSFET fabricated by a split-gate technique on an SOI substrate. This large amplitude of RTS can be understood by the numerical calculation which takes the potential of the charged trap into account.

1. Introduction

The advances in Si ULSI technology make it possible to integrate more than a million gates in one chip today. The gate length of MOSFETs reaches 0.5 μm in the production domain, and in the research domain even shorter gate lengths of 0.04 μm have been reported [1]. In such fine structures, conductance fluctuations are expected to occur at low temperatures due to quantum effects [2] or single electron effects. If the progress of device integration and miniaturization continues as at present, these effects may become a serious problem in Si ULSI because they would affect the characteristics and performances. Therefore, it is very important to investigate the electrical transport properties in such fine structures and devices. Random Telegraph Signal (RTS) is one of such conductance fluctuations arising from the capture and emission of a channel electron by a trap in the gate oxide [3]. This phenomenon causes $1/f$ noise and may limit the miniaturization of MOSFET. Although many experiments of RTS have been reported so far, their relative amplitudes ($\Delta I_{ds}/I_{ds}$) are normally less than 1% [4] and at most 30% [5]. The simple analysis indicates that relative amplitude of RTS can become 100% when the channel width is very small [6].

In this paper we report the observation of very large amplitude (90%) of RTS near the pinch off at 1.5K in a very narrow, short channel Si n-MOSFET on an SOI substrate fabricated by means of a split-gate technique. We also confirm from numerical calculation that the potential of a single trap can block almost the whole channel at weak inversion region at low temperature.

2. Device Structure and Fabrication

Figure 1 shows the top view and cross sectional view of the device fabricated in this work. A silicon on insulator (SOI) substrate prepared by the SIMOX technique was employed. The device has a dual gate structure. The lower gate is a split-gate to confine carriers by the electrostatic potential in a very narrow, short channel. The upper gate is an Al gate to modulate the carrier density in the channel. By changing the bias voltages on the two gates, it is possible to change the width and the carrier density in the channel independently.

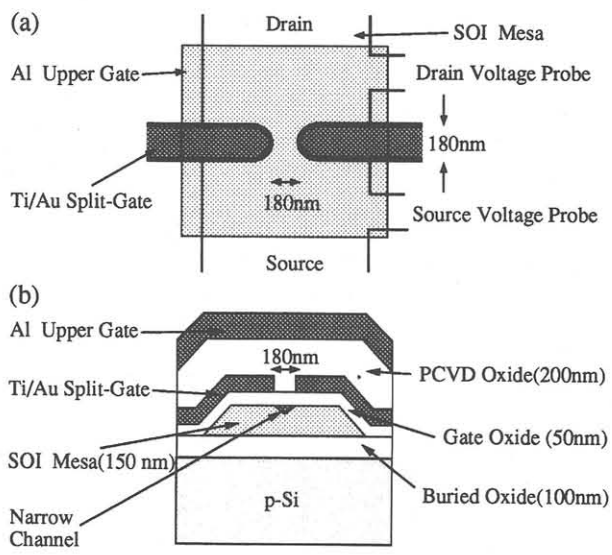

Figure 1: Schematic views of the very narrow, short channel n-MOSFET with a split-gate used in this experiment. (a) Top view. (b) Cross section.

The device fabrication steps are as follows. First, mesa isolation was formed by chemical dry etching of the thin Si layer of p-SIMOX substrate. The thicknesses of the Si layer and buried oxide are 150 nm and 100 nm, respectively. P^+ ions were implanted into the drain and source areas at 30 keV and at a dose of 10^{15} cm^{-2}. The 50 nm-thick gate oxide was then formed by thermal oxidation at 1000 °C. Electron beam lithography was used to define the lower split-gate with 300 nm-thick PMMA resist before Ti/Au was evaporated and lifted off. Both the width and length of the gap in the split-gate were 180 nm. Finally, 200 nm oxide was deposited by Plasma Chemical Vapor Deposition (P-CVD) and an upper Al gate was formed by evaporation and lift-off.

The device was mounted in a rotary pumped ^{4}He cryostat. The four terminal dc measurement by HP4156A (precision semiconductor parameter analyzer) was performed. Drain current (I_{ds}) were measured as functions of the split-gate voltage (V_{sg}) and time.

3. Experimental Results

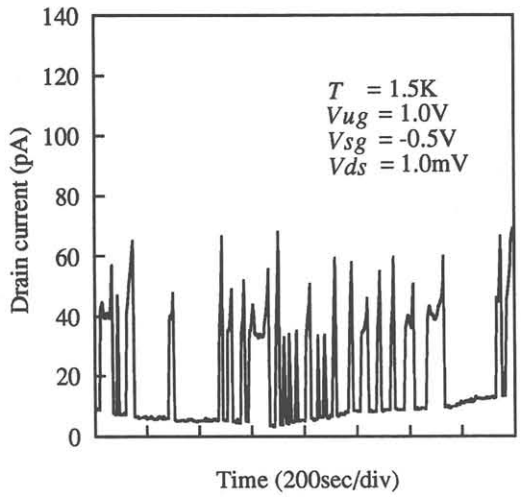

Figure 2: Time dependence of drain current at fixed gate voltage at T=1.5K. It is indicated from the signals that at least two traps are involved. While the RTS amplitude by one traps is $\Delta I/I_{peak}$ ≈80%, the current fluctuation reaches 90% by two traps.

The device shows conductance oscillations as a function of the split-gate voltage at low temperatures due to the Coulomb blockade effect [7]. Figure 2 shows the time dependence of the drain current just above the pinchoff voltage at 1.5K. The drain voltage (V_{ds}) was kept at 1.0 mV and the upper gate voltage (V_{ug}) was 1.0 V. The split-gate voltage was kept at -0.5 V. The drain current is switched between discrete levels. The distributions of the time at which the drain current is at high level or low level follow the Poisson distribution. This indicates that the switching of the drain current is caused by RTS. In this case, three discrete levels are clearly observed. This suggests that two traps exist within a short distance in the channel and affect each other [3]. The relative amplitude of the signal ($\Delta I_{ds}/I_{ds}$) is almost 80% by one trap and it becomes almost 90% by the second trap.

4. Discussions

The RTS phenomena by single electron capture and emission by the trap in the gate oxide have been extensively studied in small area MOSFET [3-6,8,9]. In this experiment, we observed very large amplitude of RTS in narrow channel MOSFET at low temperature. As the channel width becomes narrower, it can be easily anticipated that the potential of the trapped carrier can affect almost the whole channel and that the relative amplitude of RTS becomes larger. The effect of the potential would be even larger in the weak inversion regime because the screening of the potential is weak. Furthermore, the amplitude of RTS would be larger at lower temperatures because the electron have less energy.

In order to discuss more quantitatively, the RTS amplitude should be calculated. Although several authors have obtained the RTS amplitude by calculation, their models (for example, the potential form of the trapped charge) are very simple [6,8] and they are not applicable to our very narrow device. We calculated the relative amplitude of RTS ($\Delta I_{ds}/I_{ds}$) in the narrow channel as follows.

The channel conductance for the carriers with energies between $E \sim E + dE$ takes the form

$$g(E)dE = en(E)\mu(E) \times \frac{\frac{W}{L} - \frac{2r(E)}{L}}{\frac{2r(E)}{L} + (1 - \frac{2r(E)}{L})(1 - \frac{2r(E)}{W})} dE \quad (1)$$

$$g_o(E)dE = en(E)\mu(E)\frac{W}{L}dE \quad (2)$$

where $g(E)$ is the conductance with a single charged trap at the center of the channel and $g_o(E)$ is without any trap. $n(E), \mu(E)$, and $r(E)$ are carrier density, mobility, and the radius of the potential by the charged trap at energies E, respectively. W and L are channel width and length, respectively.

Integration of Eq.(1) and Eq.(2) gives the total channel conductance with and without a single trap, respectively [10]. We can obtain the relative amplitude of RTS as

$$\frac{\Delta I_{ds}}{I_{ds}} = 1 - \frac{\int_{E_C+E_o}^{\infty} g(E)dE}{\int_{E_C}^{\infty} g_o(E)dE}. \quad (3)$$

In the calculation, we assumed that the carrier mobility is equal at all energies and the carrier density is described by the Boltzmann approximation. In our device, the number of electrons participating in transport in the channel is estimated from the magnitude of conductance to be about 10. We assumed that the potential form of the trap is two dimensional screened potential [9] and that the screening parameter in this case is about 2nm.

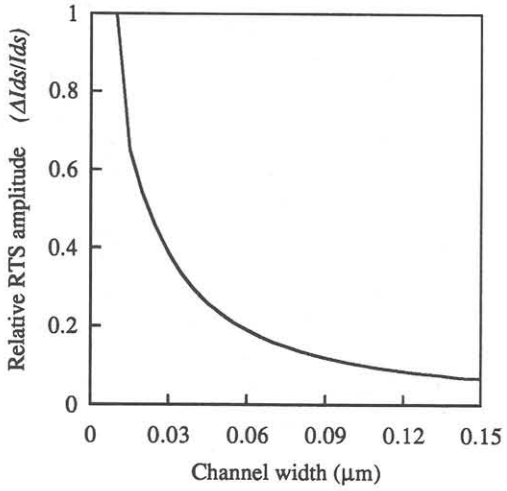

Figure 3: Calculated dependence of the relative amplitude of RTS on the channel width at 1.5K. Channel length is 300nm and screening parameter is 2nm.

Figure 3 shows the calculated dependence of the relative amplitude of RTS on the channel width. The relative amplitude of RTS becomes large rapidly with decreasing the channel width and can be larger than 80% when the width becomes less than 10nm.

In our split-gate MOSFET, the channel width is considered to be much narrower near the pinch off than the geometrical gap (180nm) of the split-gate. Furthermore, in the weak inversion regime, the channel is not only laterally confined by the split gate potential, but it could become narrower by the existence of potential fluctuations due to impurities and interface charges [11]. As a result, the channel width would easily get narrower than 10nm and only a single electron emission/capture could cause the RTS amplitude of as high as 80%.

5. Conclusions

We have observed extremely large RTS amplitude (≈90%) at low temperature in a very narrow, short channel n-MOSFET on an SOI substrate by a split-gate technique, to our knowledge, for the first time. The numerical calculation shows that in a channel narrower than 10nm, the potential of the charged trap affect almost the whole channel and the RTS amplitude becomes as high as almost 100%.

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