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The Possibility of Quantized Conductance at Temperatures above 4.2K in Bulk Si MOSFETs

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Conductance was measured in bulk Si MOSFETs, which had gates with a narrow neck in the middle. In MOSFETs with SiO_2 isolation regions, the conductance at 4.2 K showed step structures and the transconductance (derivative of the conductance) at 77 K showed periodic oscillations. This anomalous behavior may be due to the formation of two types of one-dimensional wires in the narrow-neck region configured by the SiO_2 isolation.

1. Introduction

One-dimensional (1D) quantum devices operating at temperatures much higher than 4.2 K (liquid-helium temperatures) have been extensively studied for use in compound semiconductors [1]. In silicon devices, however, observation of the clear periodic steps of the conductance is difficult even at low temperatures because of the lower mobility. A recent report on silicon wires fabricated on a SIMOX (Separation by IMplanted OXygen) wafer [2] is the only one so far claiming observation of quantized conductance at temperatures far above 4.2 K, as far as we know.

In this work, we report the results of conductance measurements in two types of bulk Si MOSFETs, the gates of which had a narrow neck in the middle. In the one type, the conductance at liquid-helium temperatures (4.2 K) showed step structures. At liquid-nitrogen temperatures (77 K), periodic oscillations in the transconductance (derivative of the conductance with respect to the gate voltage) were observed. The origins of the step structures and the oscillations are discussed in terms of 1D-subband formation in the neck region.

2. Experimental

The sample structures used in our experiments are shown in Fig. 1. Two types of n-channel MOSFETs with 4-μm-long gates (Figs. 1(a) and (b)) were examined. Both had a neck in the middle which formed a short narrow channel, as in a point-contact structure [3]. The triangular gate regions sandwiching the neck region formed the 2D source and drain regions. The threshold voltage was lower in these regions than in the neck region. This means that these regions become strongly inverted when current begins flowing in the neck region. The gate width in the neck region was 0.24 μm, and the thickness of the gate-oxide was 5 nm. Since the gate looks like a butterfly, these MOSFETs are referred to as 'Butterfly MOSFETs' or 'B-MOSFETs'.

The two types of B-MOSFETs differ in their channel configuration. The channel region in the MOSFET of Fig. 1(a) was isolated with p^+ regions, which were formed in the middle of the field region by ion-implantation using the gate as a mask. The channel region in the MOSFET of Fig. 1(b), on the other hand, was isolated with thick SiO_2 regions, the edges of which are under the gate and thus cannot be seen clearly in Fig. 1(b). The SiO_2 isolation regions were formed by single-Si_3N_4-spacer offset local oxidation [4]. The scanning electron micrograph in Fig. 1(c) shows the configuration of the SiO_2 isolation regions. In order to see this configuration, the p-substrate was etched from the back after fabrication and the micrograph was taken from the back. The SiO_2 spacing in the neck region was below 50 nm, as shown in Fig. 1(c).

The p concentration in the channel region was around $2x10^{17}$ cm^{-3}. Conventional process technologies with KrF-eximer phase-shift lithography were used for the fabrication. Current I_{ds} between the source and drain regions was measured using an HP 4145A semiconductor parameter analyzer at both 4.2 and 77 K.

3. Results and Discussions

The conductance of the two-types of B-MOSFETs at 4.2 K are compared in Figs. 2 and 3. Source-drain voltage V_{ds} was 10 mV. The I_{ds} of the B-MOSFET with p^+ isolation regions monotonously increased with an increase in gate voltage V_g, as shown in Fig. 2, although some fluctuations were observed. The I_{ds} of the B-MOSFET with SiO_2 isolation regions, on the other hand, showed anomalous behavior. Plateau A0 and periodic step structures B0, B1, and B2 can be seen.

At 77 K, transconductance dI_{ds} / dV_g of the B-MOSFET with SiO_2 isolation regions showed periodic oscillations (Fig. 4). These oscillations (denoted as C0, C1, C2, and D0) became more pronounced as substrate voltage V_{sub} became more negatively biased. Figure 5 shows the transconductance at 77 K for various V_{ds}. The oscillations continued for V_{ds} up to 100 mV.

We believe that the step structures at 4.2 K resulted from 1D subband formation in the neck region of the B-MOSFET. Since anomalous behavior has not been observed in B-MOSFETs with p^+ isolations, the oscillations were most likely caused by the narrow channel configured by the SiO_2 isolation regions with short spacing.

Figure 6 shows a schematic cross-section of the neck region. The field region bends at the edges due to the strain. Since the threshold voltage is lower at the edges than in the center in this type of structure [5], we suspect that plateau A0 corresponds to the current along the edges and that the B-series (B0, B1, and B2) corresponds to the current flowing over the entire field region. The difference in conductance between A0 and B0 may arise from the difference in the transmission coefficient between the two types of 1D wires.

The Vg spacing of 0.1 V between the B-series roughly gives a 1D confinement width of 20 nm, which is not far from the SiO_2 spacing observed in Fig. 1(c). The quantized conductance for the B-series is estimated to be $1.5 \cdot e^2/h$, if we assume series 2D resistance in the neck region [6]. This value is in fairly good agreement with the quantized conductance, $2e^2/h$, observed in compound semiconductors [3].

The origin of the oscillations at 77 K may also be related to the two types of 1D-subband formation in the neck region. The two facts have a bearing on the origin: (1) the C-series (C0, C1, and C2) appears in weak inversion rather than in strong inversion, and the corresponding I_{ds} is too small (below 100 nA) for 1D conduction; (2) the C-series seems to correspond to A0 rather than to the B-series at 4.2 K in terms of their $V_g - V_{th}$ range. The V_{sub} dependence of the C-series also indicates that they correspond to A0. As the substrate becomes more negatively biased, more oscillations of the C-series appear (Fig. 4), corresponding to the expansion of the A0 plateau (Fig. 3).

Based on these facts, we suspect that the C-series results from the occupation of the next higher 1D subband by electrons in the upper tail of the Fermi-Dirac distribution at 77 K. Non-uniform density of 1D-subband states can cause oscillations in the C-series even if the transport is not ballistic [6]. These subbands will be those formed at the edges rather than over the entire field region (at 4.2 K, the first ones result in plateau A0 and the latter ones result in the B-series).

The reason the step structures in the conductance (corresponding to C1 and C2) were not observed in the A0 region at 4.2 K is that the energy spacing for the subbands formed at the edges is much larger than kT at this low temperature, so only the lowest subband is occupied. The energy spacing can be estimated from Fig. 5. The C0 oscillation is seen for Vds up to 100 mV, at which point the source-drain voltage across the 1D neck region is estimated to be 10 mV, assuming the presence of a 2D neck region. The energy spacing between the first and second subband formed at the edges will be at least larger than this value. We also suspect that D0 at 77 K corresponds to B0 at 4.2 K.

B-MOSFETs with SiO_2 isolation regions have some advantages for observing (quasi-)1D conduction at high temperatures: (1) The 1D channel is short and narrow, as in a point-contact structure. (2) The 1D channel is far from the n^+ diffusion regions where many defects are induced by the high ion-implantation dose. (3) Strong confinement can be achieved because the potential well is formed by the inner electric field rather than by the outer edges of the depletion regions as in a point-contact structure.

4. Summary

We measured the conductance of two types of bulk Si MOSFETs, the gates of which had a narrow neck in the middle, at both 4.2 and 77 K. In MOSFETs with SiO_2 isolations, the conductance at 4.2 K showed step structures, which were attributed to 1D conduction in the rectangular cross-section neck region. The transconductance (derivative of the conductance) at 77 K showed periodic oscillations, which were attributed to 1D-subband formation in the corners of the rectangular cross-section, at a small gate voltage near the threshold voltage.

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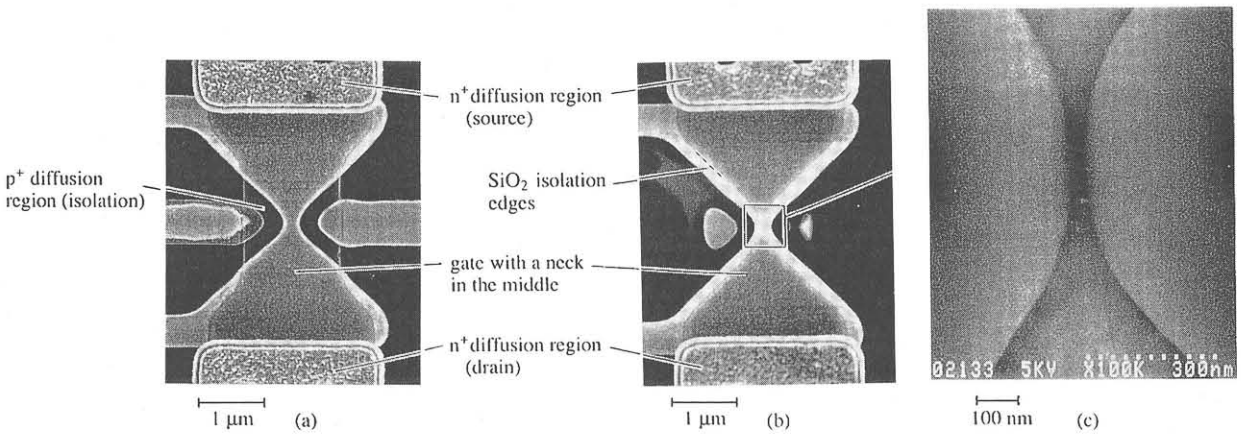

Fig. 1 Scanning electron micrograph of B-MOSFETs: (a) p^+ isolations, (b) SiO_2 isolations (which are not seen clearly here), (c) configuration of SiO_2 isolations for the B-MOSFET of Fig. 1(b).

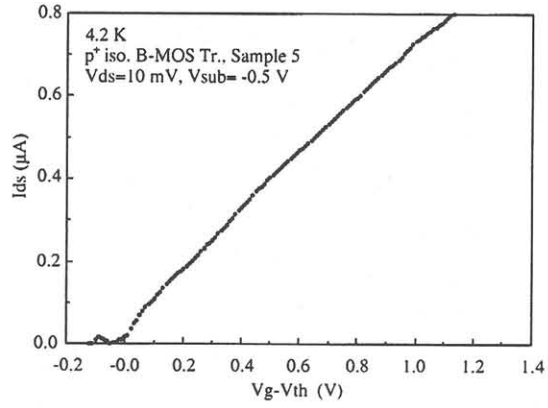

Fig. 2 Conductance of B-MOSFET with p^+ isolations at 4.2 K.

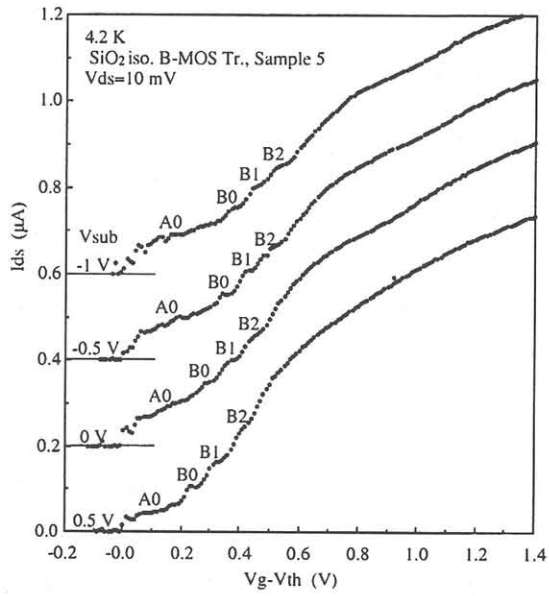

Fig. 3 Conductance of B-MOSFET with SiO_2 isolations at 4.2 K. The curves for various Vsub are offset vertically for clarity.

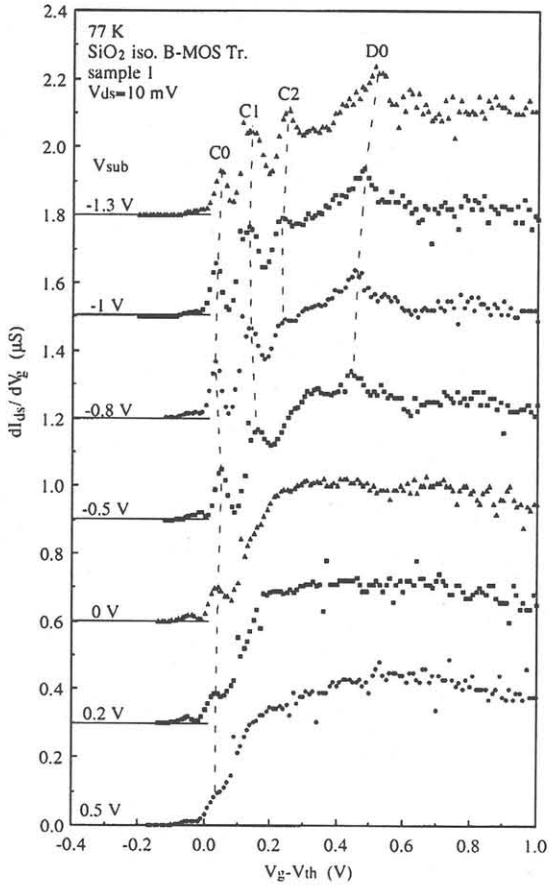

Fig. 4 Transconductance of B-MOSFET with SiO_2 isolations at 77 K. The curves for various Vsub are offset vertically for clarity.

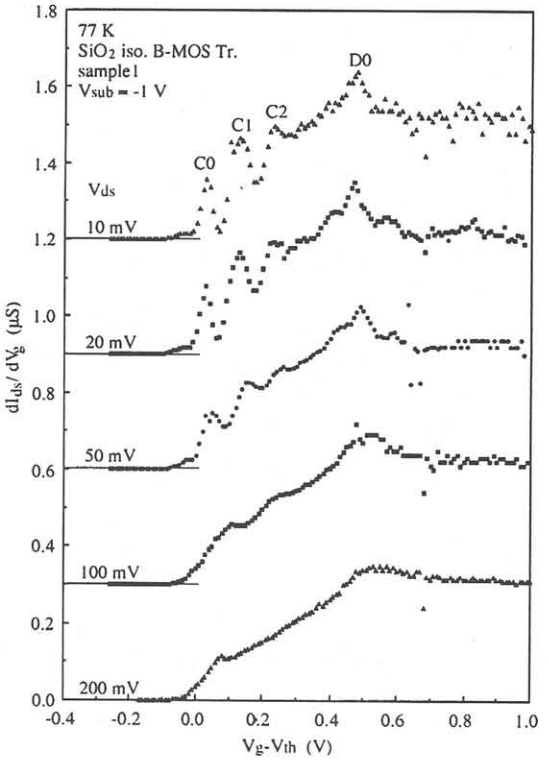

Fig. 5 Transconductance of B-MOSFET with SiO_2 isolations at 77 K. The curves for various Vds are offset vertically for clarity.

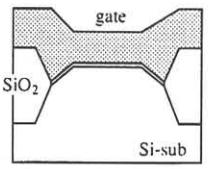

Fig. 6 Schematic cross section of B-MOSFET with SiO_2 isolations (Fig. 1(b)).