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Elimination of Al Line and Via Resistance Degradation under HTS Test in the Application of F-Doped Oxide as Intermetal Dielectrics

B. K. Hwang, J. H. Choi, S. W. Lee, K. Fujihara, U. I. Chung, S. I. Lee and M. Y. Lee
Semiconductor R&D Center, Samsung Electronics, Co Ltd.
San 24, Nongseo-Ri, Kiheung-Eup, Yongin-Kun, Kyungki-Do, KOREA
Telephone: 82-2-760-6336, FAX: 82-2-760-7991

ABSTRACT

The typical issues in the application of SiOF on IMD are as follows: (1) the increase of line resistance, (2) the wedge-like defects of metal line, (3) the stress change of film, and (4) via resistance degradation during HTS test at 350°C. The above problems in using the SiOF as IMD can be eliminated by the passivation of IMD with PE-SiN and the application of Ti underlayer before the second metal deposition.

INTRODUCTION

The shrinkage of device dimension accompanies the increase of *RC* delay. One of effective methods to reduce *RC* delay is to decrease the parasitic capacitance by appling low dielectric material in the gaps between metal lines.[1] The candidates for low dielectric materials are classified into organic polymers such as BCB, parylene, and polyimide derivatives and inorganic oxide.[2] Generally, the organic polymers have more significant problems associated with integration than inorganic oxide. But the inorganic oxides have many issues to be solved for the application in intermetal dielectric layer (IMD), too. The fluorine doped silicate (SiOF) has been considered as one of inorganic low dielectric constant materials. Recently, the behaviors of fluorine in SiOF on metallization have been investigated intensively.[3] In this paper, we propose reliability issues in double level interconnections under the high temperature storage (HTS) test and solutions about these issues.

EXPERIMENTAL

The SiOF was deposited by the parallel electrode PE-CVD system using TEOS, O_2, and C_2F_6 as source gases. The incorporation of fluorine into SiO_2 was confirmed by XPS, AES, and FTIR spectra. The tested structures for IMD were the conventional PE-TEOS ox. or SiOF / SOG etch back / PE-TEOS ox. For evaluating via and line resistance, the first metal was fixed as Ti / TiN / Al and that of second metal was splitted into Al or Ti / Al. After forming via, the passivation was made by PE-SiN. HTS test was executed at 350 C in air at the constant time of intervals. The brief process flow is shown in scheme 1.

RESULTS and DISCUSSIONS

The concentration of fluorine and dielectric constant are changed with C_2F_6 flow rates. As the C_2F_6 flow rates increase, the concentration of fluorine increase and dielectric constant decrease to ca. 75 % of normal PE-TEOS oxide as shown in figure 1. The line resistances of first metal were abruptly increased after 300 hours of HTS. The higher C_2F_6 flow rate was, the larger the increased amount of resistance was. Figure 2 shows these features. Using SiOF on IMD integration, the major problem to be overcome is to stabilize the physical properties - stress and RI. This film instability comes from the desorption of fluorine species during HTS as explained another paper.[4] After HTS test for 300 hours, the stress induced wedge-like defects at the side of metal line which might be the reason of line resistance increase were found as in microscopic picture of figure 3. We examined the stress change of SiOF films passivated by various films to solve two issues : the increase of line resistance and the wedge-like defects. Figure 4 shows the stress changes of SiOF with various capping methods

in accordance with HTS time. From this figure, it can be known that the stress of SiOF film was relatively stable in the existence of PE-SiN layer compared with SiOF only. It indicates that there is no structural change of SiOF film passivated by PE-SiN. Wedge-like defects and the increase of line resistance were not found in the application of passivation of PE-SiN as shown in figure 5.

To see the effect of barrier metal on via resistance degradation during HTS, Ti was sputtered before the second Al deposition. Figure 6 shows the effects of Ti underlayer on via resistance. Initially, the via failures were not found in all splits. Without Ti underlayer, however, almost all vias were failed even in 100 hours of HTS. In the case of existence of Ti underlayer, via degradation and failures were not found regardless of Ti thickness. It is clearly shown that Ti underlayer can keep via resistance from degradation during HTS and 300A of Ti was enough for this protecting capability. To analyze the via resistance degradation without Ti underlayer, TEM was taken at the failed via. The picture is shown in figure 7. The voids were observed in via without Ti underlayer and these voids in the via without of Ti underlayer made via resistance degradation. Voids, however, were not found in via with Ti underlayer from TEM, so stable via resistance could be obtained using Ti underlayer. In terms of via resistance degradation and failures, Ti underlayer was definitly suppressed the stress migration induced voids in metal at via side wall.

SUMMARY

Consequently, the problems in using the SiOF as IMD such as the wedge-like defects of metal line, the stress change of film, the increase of metal line resistance during HTS, and the via resistance degradation can be removed by the application of Ti underlayer before the second metal deposition and passivation of IMD with PE-SiN.

REFERENCES

1) T. Sakurai, IEEE Trans. on Electron Devices, **40** (1993) 118.
2) M. Mills, et al., Proc. of DUMIC, 269 (1995); N. Hendricks, et al., *ibid*, 283 (1995).
3) M.J Shapiro, et al., Proc. of DUMIC, 118 (1995).
4) J. H. Choi, et al., Proc. of VMIC, in press.

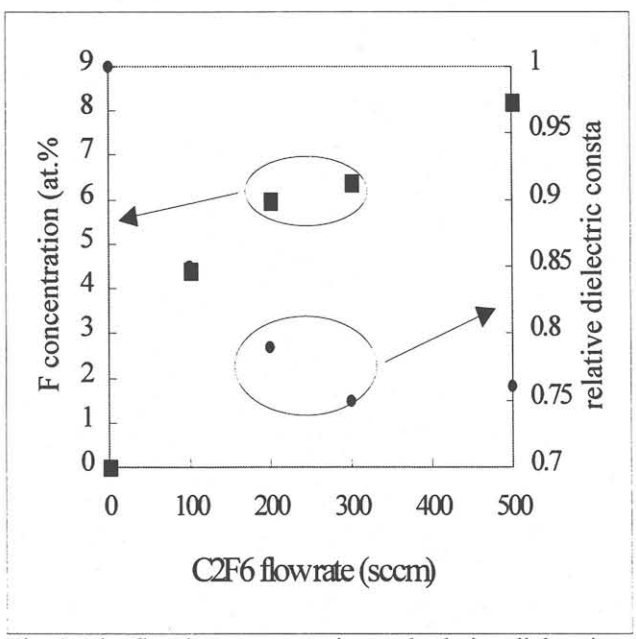
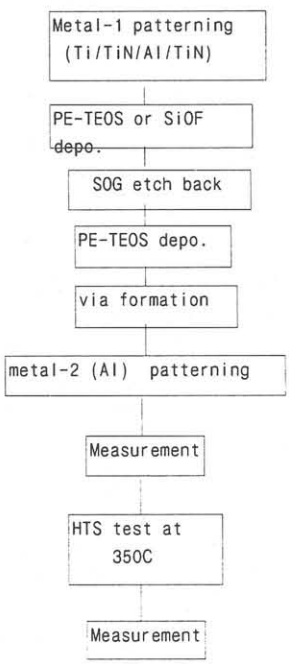


Fig. 1. The fluorine concentration and relatine dielectric constant with C2F6 flow rate.



Scheme 1. The brief process for this study.

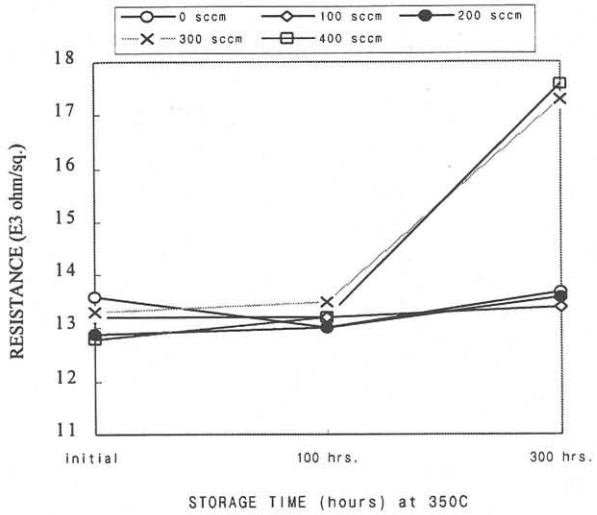


Fig. 2. The changes of line resistance for first metal during HTS test with C2F6 flow rate.

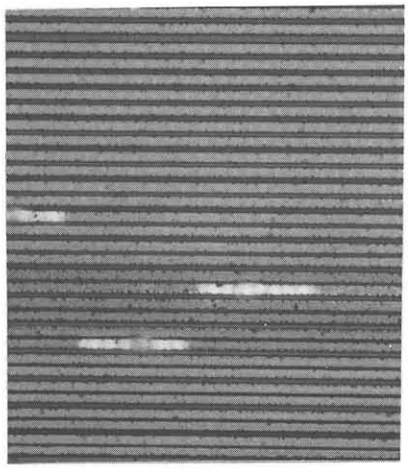


Fig. 3. The microscopic photograph showing the wedge-like defects at the side of metal lins.

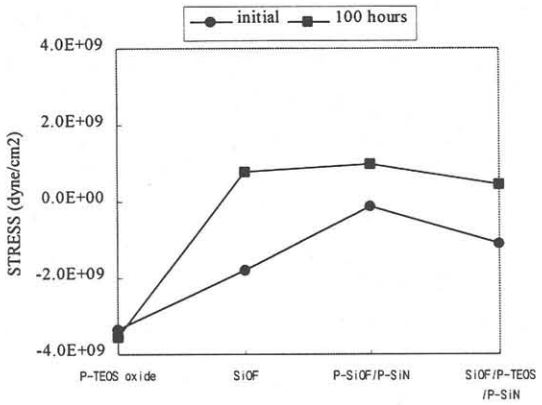


Fig. 4. The stress changes of SiOF with various capping layers during HTS test.

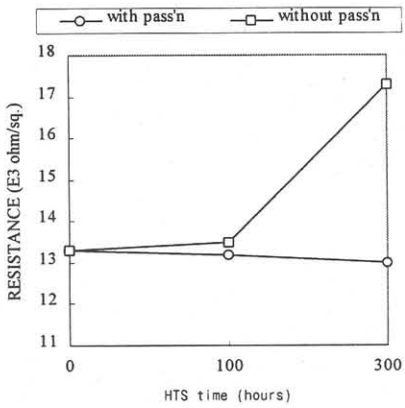
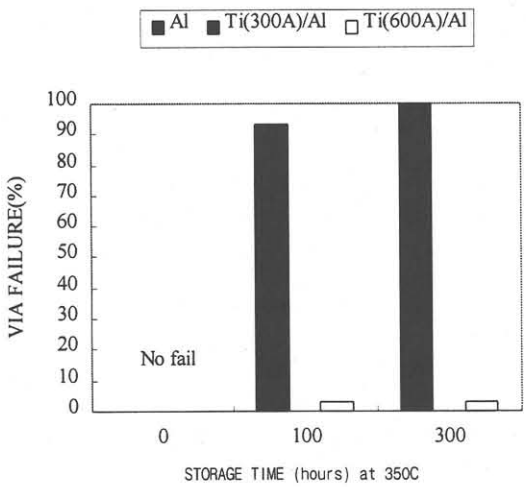


Fig.5. The changes of line resistance for first metal with or without PE-SiN passivation during HTS test.



(contact size = 0.7X0.8um @ 300sccm of C2F6)
Fig. 6. The accumulated via failures (%) showing Ti underlayer effects during HTS test.

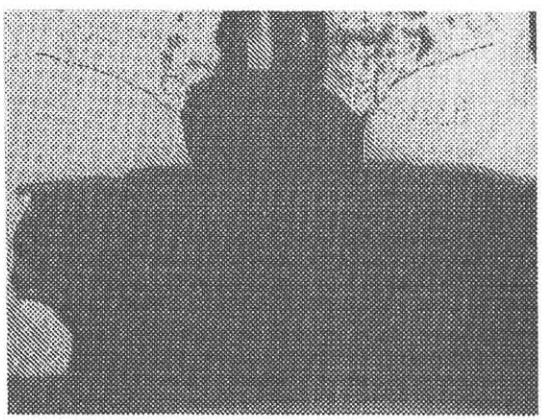


Fig. 7. TEM of failed via showing the SM-induced voids @ without Ti underlayer