

Atomic-Scale Planarization of 6-Inch Si(001) Substrate by UHV Heating

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By means of heating in ultrahigh vacuum (UHV), we obtained atomically flat Si(001) surface with wide spread reconstructed 2×1 structure on the 6-inch substrate. This planarization was accomplished by a modified RCA method as the pre-cleaning and the UHV heating. The substrate temperature could be lowered to 600°C by optimizing the pre-cleaning condition. The reflection high energy electron diffraction (RHEED) pattern indicated oxide free surface consisted of 2×1 monoatomic step structure. From cross-sectional transmission electron microscopy (XTEM), root-mean-square (rms) roughness was less than 0.1 nm almost all over the 6-inch substrate.

1. Introduction

Atomic-scale planarization of Si surfaces has become a key issue for the ULSI processing. This is because the mobility of electrons within the inversion layer and the dielectric breakdown characteristics strongly depend on the surface microroughness^{1,2}. Recently, planarization of Si surfaces has been extensively studied by a wet treatment^{3,4}.

On the other, an atomic-scale planarization of the small pieces of Si(001) substrate by heating in ultrahigh vacuum (UHV) has been investigated^{5,6}. From a practical point of view, it is required to planarize a Si surface by a wafer size. In this paper, we report on an atomically flat surface formation of 6-inch Si substrate using a newly developed UHV system.

2. UHV system

Figure 1 shows the UHV system newly developed for the planarization of 6-inch Si substrate. This system consists of three chambers i.e., a cleaning, a preheating, and a load-lock. This system was evacuated by turbomolecular pumps, ion pump, and titanium sublimation pumps. A base pressure of 3×10^{-9} Pa has been attained in this system. Infrared heating as well as tantalum resistive heating were introduced for the substrate heating. Temperature on Si substrate surfaces was measured by thermocouples and pyrometer. A reflection high energy electron diffraction (RHEED) was equipped in the cleaning chamber.

Both in the cleaning and in the preheating chambers, aluminum radiation shields were used to suppress the elevating temperature of the chamber walls by reflecting radiant heat from a substrate heater. By using this radiation shield, it has become possible to heat the 6-inch

substrate at above 700°C under a pressure of 10^{-8} Pa order in the cleaning chamber.

3. Experimental

In this experiment, p-type, 6-inch Si(001) substrates ($\rho=5-10\ \Omega\text{cm}$) were used. At first, the substrates were treated by a wet chemical process. As the wet chemical process, a modified RCA cleaning as well as SC-1 cleaning was investigated.

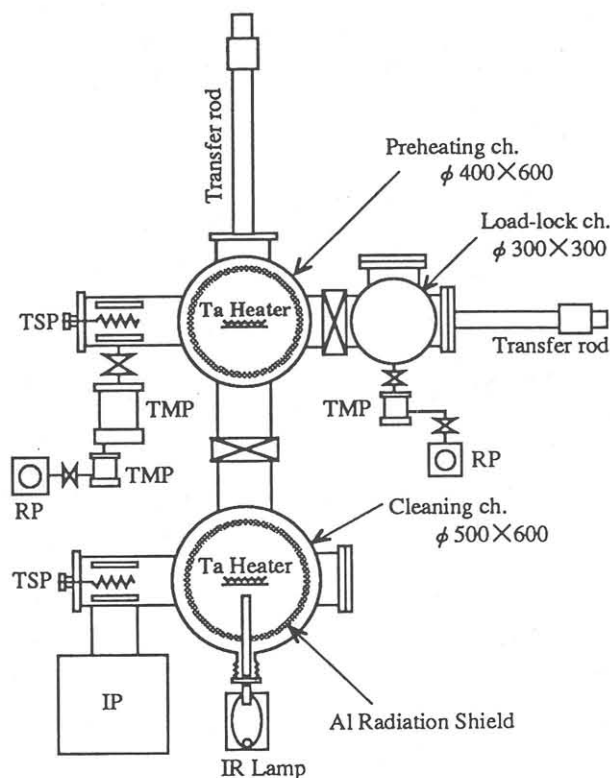
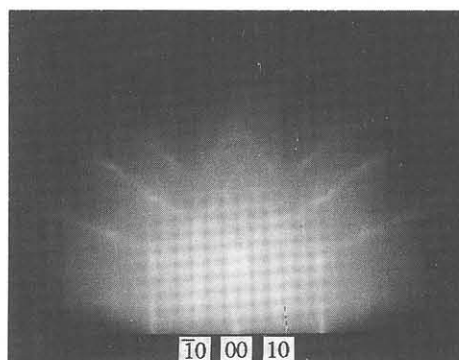


Fig. 1 Configuration of the UHV system

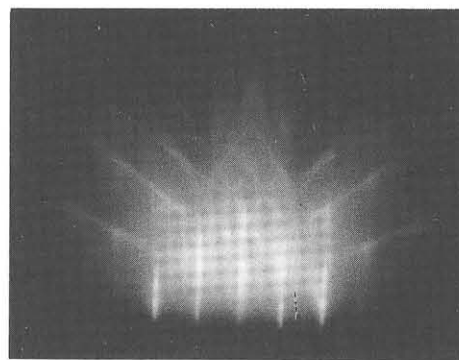
The modified RCA cleaning consists of three steps, i.e., wet treatment by 1) SC-1 where $\text{H}_2\text{O}_2 / \text{NH}_4\text{OH}$ ratio is increased, 2) Diluted HF solution and 3) SC-2. The modified RCA cleaning was performed at room temperature. After these wet chemical treatments, the substrates were introduced into the UHV system and heated in the cleaning chamber. Si surface structure was

observed by the RHEED with an acceleration voltage of 29kV. Incident direction of primary electron beam was $\langle 110 \rangle$.

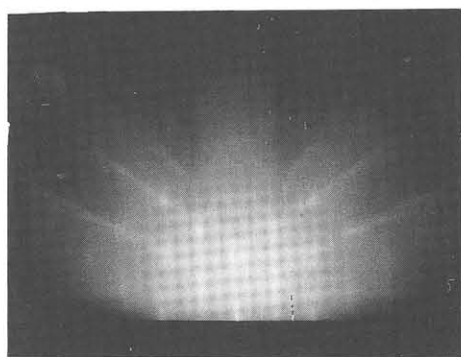
Si surface roughness was observed by cross-sectional transmission electron microscope (XTEM). Polysilicon was deposited on the surface as a cap layer for the XTEM sample. Root-mean-square (rms) roughness was evaluated



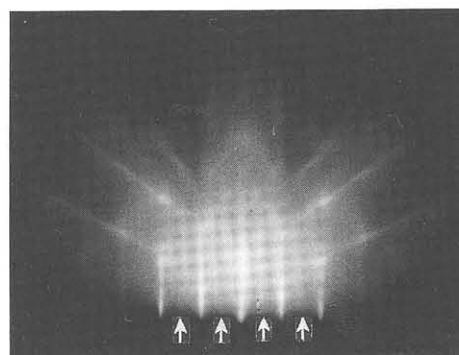
(a) Room Temperature



(d) Room Temperature



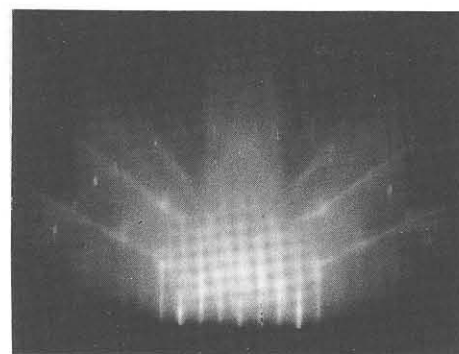
(b) 585°C, 12hours (in-situ)



(e) 585°C (in-situ)



(c) 785°C, 1.5hours (in-situ)



(f) 600°C, 90hours (in-situ)

Fig. 2 RHEED patterns from 6-inch Si(001) substrate.
(a)-(c) from substrate treated by SC-1. (d)-(f) from substrate treated by modified RCA cleaning.

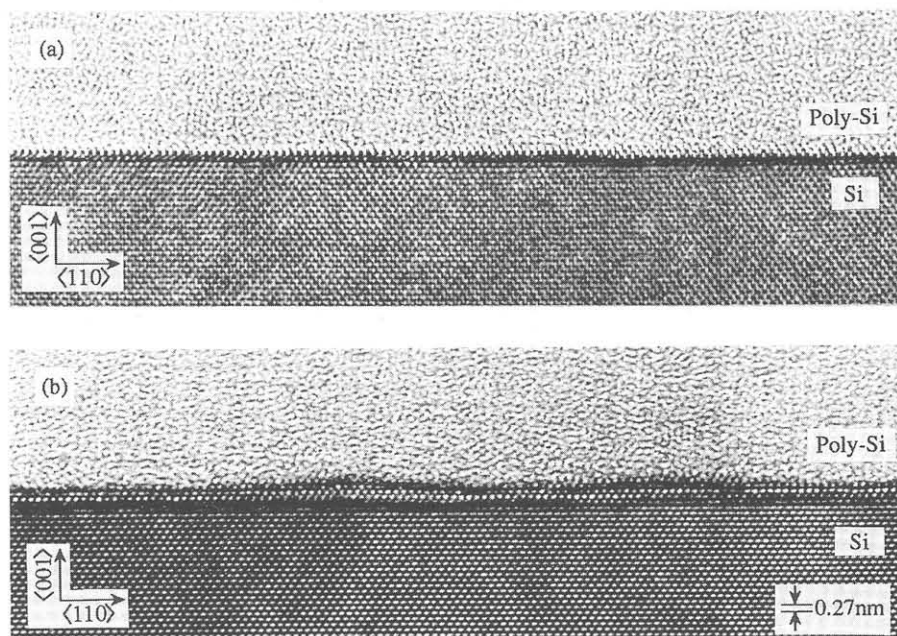
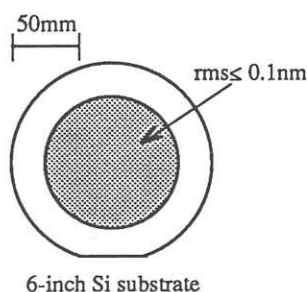


Fig. 3 XTEM image of Si(001) substrate (a) heated at 600°C in UHV after the modified RCA cleaning and (b) treated by SC-1 cleaning. The left side of (a) shows the planarized area with rms roughness of less than 0.1nm.

by a digitization of the lattice site at the oxide-Si(001) interface boundary.

4. Results and Discussion

Figure 2(a)-(c) show RHEED patterns from the Si surfaces prepared by SC-1 cleaning prior to UHV heating. On the other, Fig. 2(d)-(f) show RHEED patterns from the Si surfaces prepared by the modified RCA cleaning prior to UHV heating. As shown in Fig. 2(a) and 2(d), RHEED pattern revealed 1×1 structure for both types of the surface. The surface structure converted from 1×1 to 2×1 depending on elevating temperature, during UHV heating. For the modified RCA cleaned surface, 2×1 structure began to reveal at 585°C[Fig.2(e)], and clear 2×1 reconstructed structure was obtained at 600°C[Fig.2(f)]. The 2×1 pattern with sharp streaks indicates the oxide free reconstructed clean surface. No surface contaminated structures like SiC were observed. On the other, 2×1 pattern could not observed at all at 585°C for SC-1 cleaned surface[Fig.2(b)]. Finally, the 2×1 structure was obtained at 785°C[Fig. 2(c)].

Figure 3(a) shows the XTEM micrograph of the 6-inch substrate heated at 600°C in UHV after the modified RCA cleaning. The rms roughness was at most 0.1 nm within the observed micrographs. And from numerous XTEM observations, it has become clear that the rms roughness of almost all the area on the substrate was less than 0.1nm (shaded area in left side of this figure). No dislocations were generated on the surface at all. From these considerations, it was clarified that the atomic-scale planarization was realized within a whole practical area for device fabrication. In contrast, as indicated in

Fig. 3(b), the XTEM micrograph of the 6-inch Si substrate treated by the SC-1 cleaning showed rough surface in comparison with the UHV heated surface.

5. Conclusion

In conclusion, the heating in UHV after the modified RCA cleaning provides a practical method for the atomic planarization of the large diameter Si substrates.

This atomic-scale planarization was realized at relatively low temperature(600°C) under a pressure of less than 7×10^{-8} Pa

Acknowledgments

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