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Effects of Channel Thickness on Poly-Crystalline Silicon Thin Film Transistors

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The effects of channel thickness on poly-crystalline silicon (poly-Si) thin film transistors (TFTs) are studied. Thin poly-Si film generally consists of small grains and contains many defects. The small value of the threshold voltage (V_{th}) appearing in thin film can improve the electrical properties of the corresponding TFTs. When the film is extremely thin, it possesses very many traps, which prevent the V_{th} value from further decreasing. The way that thickness affects film quality differs according to how that film was prepared. Therefore, different TFT fabrication methods make the optimum channel thickness different.

1. Introduction

Polycrystalline silicon (Poly-Si) thin film transistors (TFTs) are certainly devices of great importance in today's microelectronics technology, since they are very useful not only in integrated circuits but also in flat panel displays. Continuous electrical improvements in poly-Si TFTs are widely required and have been actively studied both from the structural and the processing viewpoints. The high quality of channel poly-Si film is, of course, preferable for obtaining good poly-Si TFTs. Super-thin channels, for example 20 nm-thick film, are also reported to be good for poly-Si TFTs[1),2)]. This is theoretically true for a device such as a silicon-on-insulator (SOI), in which the silicon film is fairly uniform along its thickness. It, however, does not seem to be always true for poly-Si TFTs[3),4)]. Therefore, this paper would like to discuss in detail the effects of channel thickness on poly-Si TFTs which are fabricated differently from each other; namely, TFTs fabricated through high temperature process (high temperature TFTs) and TFTs prepared through low temperature process (low temperature TFTs).

2. Experiment

TFTs possessing various channel thicknesses are fabricated both through high and low temperature processes. High temperature TFTs have a staggered-type self-aligned structure. Intrinsic channel poly-Si films having thicknesses of between 19.3 nm and 167.8 nm are prepared by low pressure chemical vapour deposition (LPCVD) at 600° C to a thickness of between 76 nm and 218 nm followed by gate oxidation at 1160° C. The oxide thickness is around 123.6 nm. Phosphorus doped n^+ poly-Si film serves as a gate electrode. Source and drain regions have been formed by phosphorus ion implantation and subsequent activation at 1000° C. Therefore, the maximum processing temperature after poly-Si deposition is during the gate oxidation at 1160° C, which is high enough to improve the poly-Si film property.

Low temperature TFTs have a staggered-type non-self-aligned structure. Channels with the thickness of between 10.9 nm and 95.6 nm are intrinsic as-deposited poly-Si films prepared by infra-low pressure CVD (ILPCVD)[5)] at 600° C and 1 mTorr. An electron cyclotron resonance plasma enhanced CVD (ECR-PECVD) forms 148.0 nm-thick gate oxide (SiO_2) at 100° C. The gate electrode is a 200 nm layer of indium tin oxide (ITO) sputter-deposited at 150° C. The maximum processing temperature after poly-Si deposition occurs during drying at 300° C, which is low enough to keep the as-deposited film consistent.

Film properties are examined by some physical analyses, such as Raman spectroscopy, x-ray diffraction (XRD), transmission electron microscopy (TEM), and scanning electron microscopy (SEM).

3. Results

The effect of channel thickness on the source drain current (I_{ds}) during the transistor on state (ON-current) differs between high temperature TFTs and low temperature TFTs (Fig.1). The ON-current of low temperature TFTs reaches a maximum value at a thickness of about 25 nm, while ON-current of the high temperature TFTs increases continuously as it decreases in thickness. This difference between high and low temperature TFTs is explained by the different behaviour of their threshold voltages (V_{th}) and mobilities. The dependence of V_{th} on thickness is shown in Fig. 2, in which the V_{th} value does not have a simple positive correlation with channel thickness, especially in low temperature TFTs.

Two types of mobility are calculated, one using the Levinson's formula[6)] and the other using gradual channel approximation in the saturation region (Fig. 3). Figure 3 together with Fig. 2 indicates that the major cause of ON-current

increase is V_{th} decrease in thin channels.

Results of Raman measurement are drawn in Fig. 4, and total XRD intensities, which are sums of {111}, {220}, and {311} signals, are plotted in Fig. 5. Both figures reflect the degree of crystallinity of the poly-Si film. High temperature film has higher crystallinity than does low temperature film. Thicker film has generally higher crystallinity both for high and low temperature processes. For the low temperature process, the film must improve in quality while the film is growing in the LPCVD chamber, since these measurements were performed on the as-deposited films.

Crystalline grains also strongly depend on the film thickness as well as on the preparation method. Figure 6 shows the relation between the film thickness and the average grain size measured by SEM observation. The grain size is in proportion to the logarithm of film thickness both in high and low temperature films. TEM observation shows that low temperature films of 20 nm or less are not in a continuous film state but in a closely-packed island-like state and that crystalline fragments seem to coexist with amorphous fragments in the low temperature films of less than 60 nm.

4. Discussion

J. Y. W. Seto suggested that the Levinson's mobility is linearly proportional to the grain size[7]. The high temperature film in Fig. 6 and the TFT in Fig. 3 seem to support his suggestion. At the very least, the Levinson's mobility has a strong positive correlation with the grain size. Since the thin film generally consists of small grains, it must have a smaller mobility value than does the thick film. The preparation method of poly-Si film changes the degree to which grain size depends on the thickness; therefore, the degree to which mobility depends on the thickness will also change. Figure 3 shows that the Levinson's mobility of high temperature film is more sensitive to the thickness than that of low temperature film.

TEM observation shows that thin low temperature films, of a thickness less than 25 nm, contain voids and that even thinner films, typically less than 20 nm, are in a separate island-like state. It has been already reported that mobility value degrades when poly-Si film is in a separate island-like state[8]. This is the reason that a low temperature TFT decreases in mobility value when it is less than 20 nm-thick, as shown in Fig. 3.

The electrical improvement that appeared in thin films is mainly due to the small V_{th} value. Thin film generally makes V_{th} value small, though this mechanism does not always work in TFTs. If the film quality is uniform throughout its thickness and if the film is thin enough that the whole channel area is depleted, then the V_{th} value is in linear proportion to the thickness. This, however, is not the case for TFTs, because a thin poly-Si film has poor quality compared with a thick film. This is especially true for low temperature film. It is quite natural that poly-Si film with poor crystallinity possesses many defects which increase V_{th} value. The threshold voltage behaviour of low temperature TFTs shown in Fig. 2 is, thus, explained as follows: as a film decreases in thickness, the degradation of crystallinity (Fig. 4 and Fig. 5) increases the number of traps which act as accepter ions. The speed of degradation accelerates as the film loses its thickness. 19.3 nm thin high temperature film has such high crystallinity (Fig. 4 and Fig. 5) that the thin film effect of the fast formation of the inversion layer still works well (Fig. 2). There must be, however, a critical thickness, i.e. some point thinner than 19.3 nm, at which film degradation cancels the thin film effect on the threshold voltage. Below the critical thickness, the film degradation will overcome the thin film effect even in high temperature TFTs so that the ON-current will be maximum at some point thinner than 19.3 nm as observed in the low temperature TFTs in Fig. 1.

5. Conclusion

Thin poly-Si TFTs generally show better electrical properties than do thick ones. This is mainly because the threshold voltage of thin poly-Si TFTs is lower than that of thick poly-Si TFTs. However, the quality of thin poly-Si film is not as good as that of thick film. As the film decreases in thickness, the deterioration of film quality is accelerated. As long as the quality is not worsened dramatically by thinning the film, the V_{th} value of thin film is lower than that of thick film. In contrast, when thin film quality is remarkably inferior to that of a thick film, the thin film effect on V_{th} no longer works. Since the relationship between film quality and thickness depends on the preparation method of poly-Si film, the optimum thickness differs from film to film in accordance with the TFT fabrication method.

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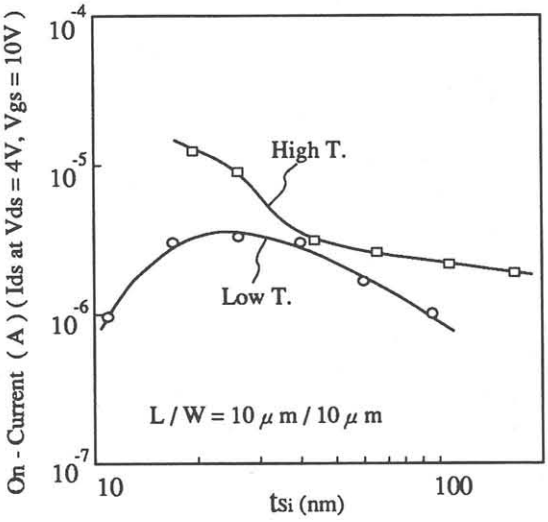

Fig. 1

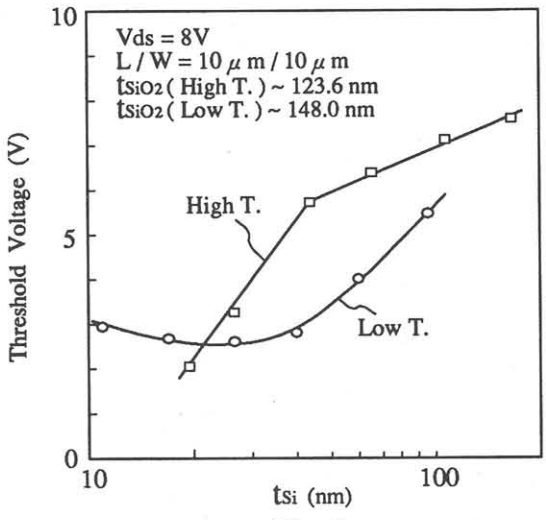

Fig. 2

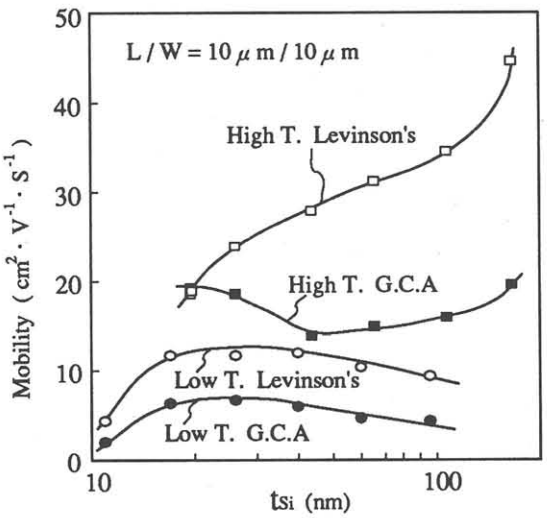

Fig. 3

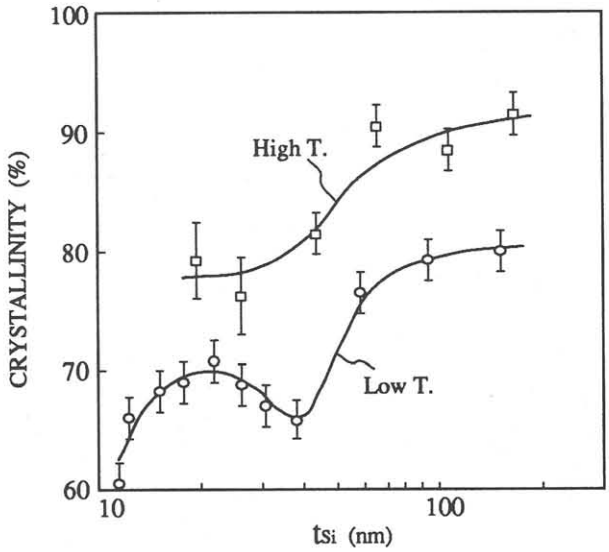

Fig. 4

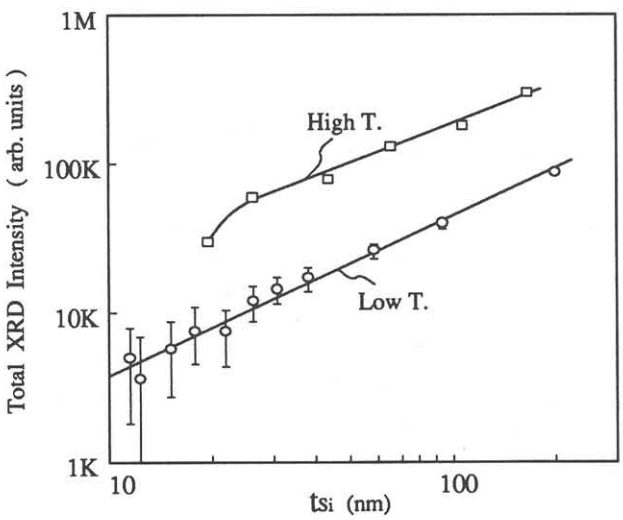

Fig. 5

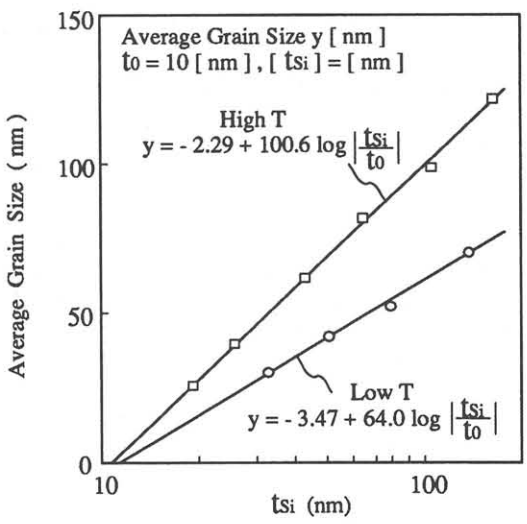

Fig. 6