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Back-Gate Effects of Amorphous-Si TFTs with an Inorganic Black Matrix on Array

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The characteristics of amorphous-Si bottom-gate thin film transistors (TFTs) with an inorganic black matrix (BM) on array for a liquid crystal display (LCD) have been investigated with various BM resistivities. High off current and large Vth shift were observed in Id-Vg characteristics because of the charge-up when the BM resistivity is as low as ~1 × 10^{12} Ω/□. When the BM resistivity is higher than the order of 10^{13} Ω/□, such severe back-gate effects were not observed.

1. INTRODUCTION

Amorphous silicon (a-Si) thin film transistor (TFT) liquid crystal displays (LCD) comprise a large portion of the flat panel display market. The requirements for TFT-LCDs include low power dissipation, low weight, and low cost for portable applications. One of the ways to lower power consumption is to increase the aperture ratio of the TFT array so that backlight power can be lowered to achieve the same LCD brightness. Use of a black-matrix (BM) on TFT array is one of the very effective methods for obtaining a higher aperture ratio. Yamanaka et al. have succeeded in applying a photo polymer BM to a TFT array.[1, 2] However, a thinner inorganic BM film with a high optical density is desirable for high quality LCDs made with fewer photolithography and etching process steps for lowering the cost. As a preliminary study of BM on TFT array we investigated the effect of BM film resistivity on TFT characteristics.

2. EXPERIMENT

A few kinds of inorganic amorphous "quasi-BM" films were deposited by DC magnetron sputtering on top of the SiNx passivation layer of conventional bottom-gate a-Si TFT test devices, as shown in Fig. 1. After the deposition of BM on TFT devices, photolithography and dry etching process were used to open the electrode pads. Several patterns of the BM on the devices were made to see the effect of wiring from the pads to the TFT. Some typical patterns are shown in Figs. 2.

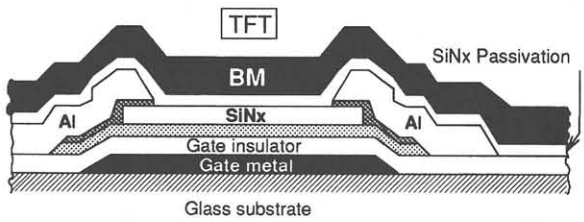

Fig. 1 Black matrix (BM) on a bottom-gate TFT test device. Cross section of the TFT part.

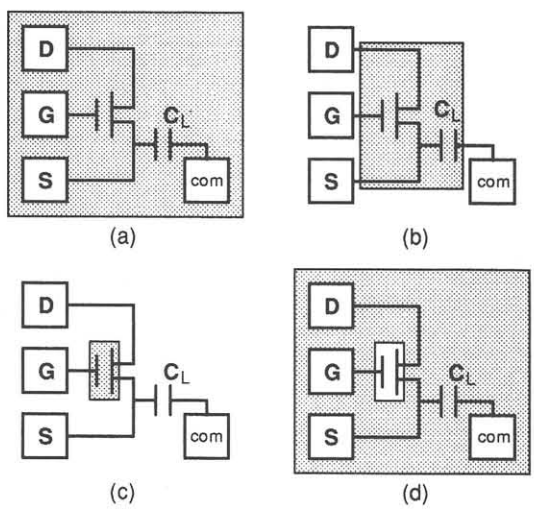

Fig. 2 Typical BM patterns (shaded part) on TFT test devices. D, G, S, and com is drain, gate, source, and common voltage pads, respectively. C_L is a pixel capacitor.

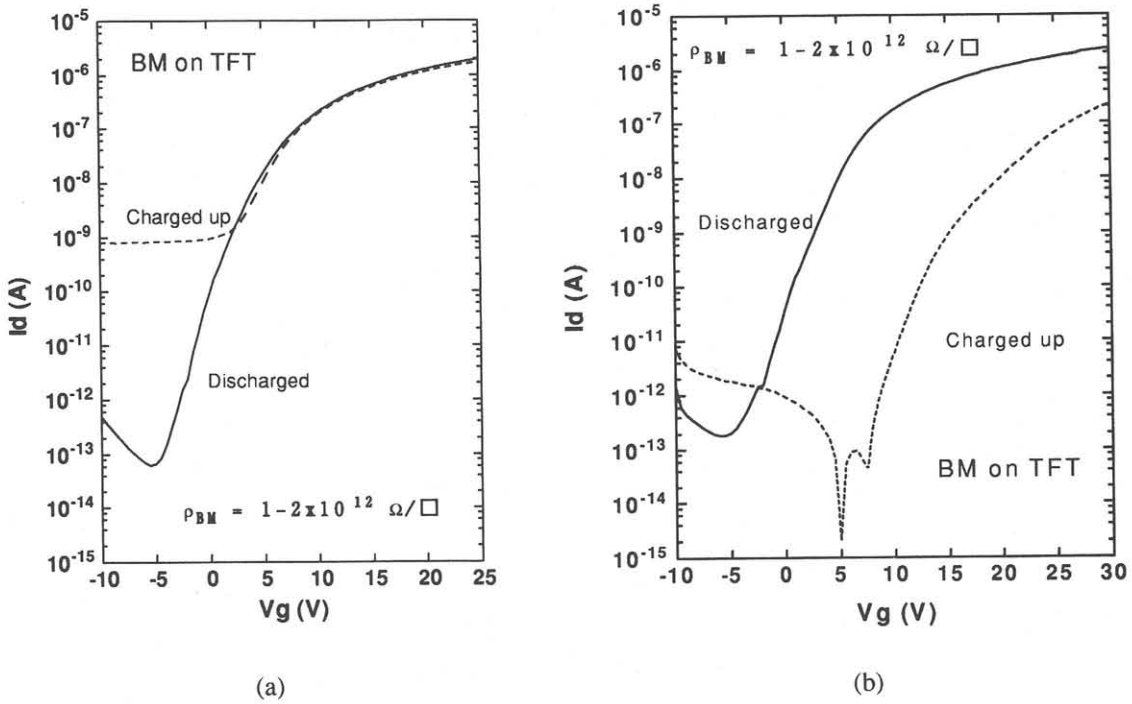

Fig. 3 Back-gate effects of BMs on TFTs due to charge up of the BMs. Vd = 10 V. The TFTs show (a) large high off current and (b) large Vth shift when the BMs are charged up.

A few kinds of surface treatment of SiNx passivation layer were also tried before depositing the BM to see the influence to the charging condition for the different kinds of interfaces. The surface treatments were such as O_2 or H_2 plasma exposure or depositing a thin SiOx layer of 150-200 Å on the SiNx passivation layer.

The BM resistivities varied from the order of 10^7 to 10^{14} Ω/□ with film thicknesses between 50-500 nm. W/L of the TFTs was approximately 19μm / 13 μm (=1.46). Conventional drain current versus gate voltage (Id-Vg) characteristics of the a-Si TFTs was measured using an HP4140B pA meter / DC voltage source. Field effect mobilities, μ, and threshold voltage, V_{th}, were determined from the saturation region of $Id^{1/2}$ versus Vg plotting. μ of the TFTs without BM were about 0.6-0.7 cm^2/Vs and the V_{th} were about 3-4 V.

3. RESULTS AND DISCUSSION

Figures 3(a) and 3(b) show typical Id-Vg characteristics of the a-Si TFT test devices with BMs on the top. As is seen in Fig. 3(a) under same conditions, a considerable high off current was observed on the same device when the BM resistivity is as low as ~2×10^{12} Ω/□. Similarly, Vth also shifted about -2 to +18 V maximum in other samples. One of the examples is shown in Fig. 3(b). When the samples were discharged by blowing with the ionized N_2 blow gun or grounded for many hours, this high off current and large Vth shift changed back to a normal low off current and Vth, respectively. The BM layers were electrically floated; therefore, these phenomena appear to be due to the BM film electrostatically charging up.

When the electrostatic voltage was measured by an electrostatic volt meter, high resistivity materials such as LCD glass substrates as well as the BM and other insulating films could charge up to about 2 or 3 kV naturally while leaving them in a clean room. This static electricity could be released easily by blowing with the ionized N_2 gun. It seems that these charges accumulating in the BM film induced the back-gating effects of the TFT which opened the channel inducing the high off current, or caused a large Vth shift.

When the BM resistivity is near the "intermediate" value such as the order of 10^{12} Ω/□ as described above, it seems that the charges can move and accumulate easily, and then trapped in the BM. When the "quasi-BM" is metal like or when its resistivity is much lower as the order of 10^7 Ω/□, no charging behavior was observed in the Id-Vg

characteristics. It appears that the charges move easily and cannot accumulate. Similarly, when the BM resistivity is higher than the order of 10^{13} Ω/□, such high off current and large Vth shift were not observed, either. These facts suggest that the back-gating effects occurred due to the electrostatic charges accumulating in the BM layer when the BM resistivity is in the "intermediate" region such as the order of around 10^{12} Ω/□ where the charges can accumulate and be trapped easily.

There was no difference in the TFT characteristics when the BM patterns are varied as are shown in Fig. 2(a), 2(b) and 2(c). The high off current and the large V_{th} shift in Id-Vg characteristics were still observed in all three BM pattern cases. The TFT characteristics of the pattern in Fig. 2(d), which has no BM on TFT, was normal and the same as that of the TFT without BM. Therefore, BM on the wirings had no influence on the high off current in Id-Vg characteristics. It appears to be that the back-gating effects were caused by the BM itself and not by the leakage current among the wires.

Difference in the interface treatment conditions also basically had no large influence to the high off current and large Vth shift in the Id-Vg characteristics. These facts also suggest that the back-gating effects are basically caused by the charging up of BM when the resistivity of BM is in the "intermediate" region, and not by the interface conditions.

As it is well known, however, that the a-Si TFTs with the BM on the top have no photosensitivity because BM blocks the light coming from the top. DC characteristics in the dark did not change even under the illumination of the room light. In the same manner, BM is also effective during the dry etching because BM can protect the TFT from exposure to the plasma as well. In the final process of TFT array it is often necessary to anneal the TFTs to recover them from the damage of plasma during the dry etching when opening the pixels and pads part which were covered by the passivation layer. However, when the BM is on the TFT, it was found that the annealing for recovering the TFT was not necessary since the BM can also protect the TFT from the plasma during the dry etching.

4. CONCLUSION

According to Id-Vg characteristics of the TFTs with the BMs on the top, it was found that there were severe back-gate effects when the BM resistivity was as low as ~1×10^{12} Ω/□. When the BM resistivity was above the order of 10^{13} Ω/□, there were no high off current or large Vth shift characteristics. The inorganic BM with resistivity above the order of 10^{13} Ω/□ is an attractive candidate for BM on array TFT-LCDs. We conclude that the higher the BM resistivity, the better the characteristics of TFT. BM is also useful for protecting the TFT from the room light as well as from the plasma during the dry etching.

ACKNOWLEDGMENT

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References

1) H. Yamanaka, T. Fukunaga, T. Koseki, K. Nagayama, T. Ueki, SID '92 Digest, pp. 789-792 (1992).

2) T. Koseki, H. Yamanaka, T. Ueki, M. Nayuki, M. Honjo, T. Minamiyama, A. Arai, in Proceedings of the Display Manufacturing Technology Conference, Santa Clara, 1995 (SID, California 1995), pp. 107-108.

3) N. S. Caswell, Japan Display '92 Digest, pp. 221-223 (1992).