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Self-Aligned Offset Gated Poly-Si TFTs by Employing a Photo Resistor Reflow Process

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We propose a new fabrication process for poly-Si TFTs with a self-aligned offset gated structure by employing a photo resistor reflow process. The new fabrication method makes the gate oxide over the offset region with an assistance of subgate and reflowed photo resistor. The new method does not require any additional offset mask step and the self-aligned implantation is applicable so that the symmetrical offset length is easily obtained.

1. INTRODUCTION

A large leakage current may be one of the critical issues for poly-silicon thin film transistors (poly-Si TFTs) for LCD applications. In order to reduce the leakage current of poly-Si TFTs, several offset gated structures have been reported. [1), 2)] In the most proposed offset structures, an additional photo lithographic step is usually required to fabricate an offset structure. The different offset length is occurred due to misalignment problem. The offset length of the source region is not same as that of the drain region so that those devices exhibit the asymmetric electrical performances such as the threshold voltage shift and the variation of the subthreshold slope. [3), 4)]

In this paper we propose a new fabrication method for poly-Si TFTs with a self-aligned offset gated structure by employing a photo resistor reflow process. The proposed device is designed to employ the gate pattern to define the offset region so that the process does not require any additional mask step and eliminates the misalign problem. In the proposed device, the self-aligned implantation is applicable so that the offset length of the source is identical with that of the drain.

2. DEVICE STRUCTURE

A schematic structure of the proposed device is illustrated in Fig. 1. The gate structure of the proposed device consists of two parts rather one in the conventional device. As shown in Figure 1, we entitle the main gate where the gate bias is applied and the other is the entitled subgate which is separated from both sides of the main gate. The gate oxide of the new device is expanded to the subgate adjacent to the source and drain. We define the expanded part of the gate oxide as the offset oxide. The poly-Si channel layer below the offset oxide is protected from the injected ion impurities for the source/drain implantation. Because the subgate is not connected to any electrode, the gate bias is not applied to the subgate. The poly-Si channel layer below the offset oxide acts as an offset region of the proposed device. The offset length of the device is sum of the subgate length and the space of the subgate and the main gate.

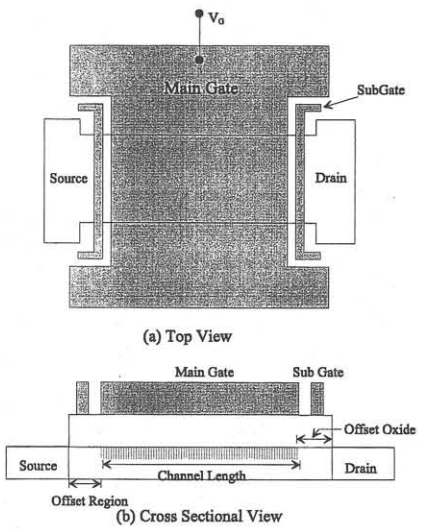

Fig. 1 The schematic view of the proposed TFT
(a) Top view (b) Cross-sectional view

3. FABRICATION PROCESS

The process sequences to form the offset oxide is illustrated in Fig. 2. A 100nm thick poly-Si film was a deposited by low-pressure chemical vapor deposition

(LPCVD) on a 500nm wet oxidized silicon wafer. A 100nm-thick gate oxide insulator is deposited by an atmospheric pressure chemical vapor deposition (APCVD). Then, a 200nm-thick gate poly-Si film is deposited by LPCVD. In order to pattern the poly-Si gate, the poly-Si film is etched out by RIE. The photo resistor is reflowed at 160 ^oC for 30 minutes (Fig 2(c)) and gate oxide is etched out (Fig. 2(d)), which is followed by the removal of the photo resist (Fig. 2(e)). During the poly-Si gate etch, the oxide between the main gate and the subgate is not etched due to the reflowed photo resist which is filled in the space between the subgate and the main gate. For the source and drain implantation, the ion impurities are not injected into the poly-Si active layer below the offset oxide.

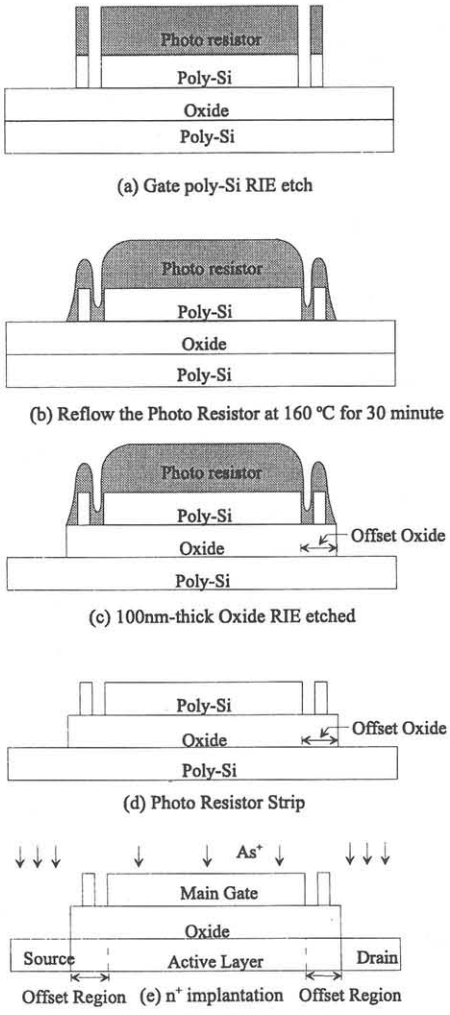

Fig. 2 The key processes for fabricating the offset oxide.

Figure 3 shows a cross-sectional SEM image of the oxide fabricated by photo resistor reflow method. The space between the main gate and the subgate is 0.5μm, and subgate length is 0.8μm of offset oxide in SEM image of Fig. 3. In our experiment, the space between the main gate length is varied from 0.2μm to 0.8μm and the subgate length is varied from 0.3μm to 1.2μm respectively. The uniform offset oxide layer is formed at both sides of a poly-Si main gate. We have verified the existence of the offset oxide by SEM. The offset length of 0.5μm to 2.0μm is obtained successfully.

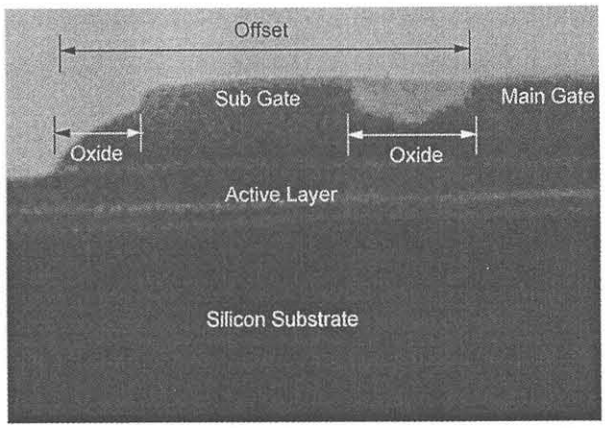

Fig. 3 The SEM image of offset oxide. The space between the main and the subgate is 0.5μm, and subgate length is 0.8μm

4. SIMULATION RESULTS AND DISCUSSION

We have verified the feasibility of our new fabrication process by SUPREM IV and the SILVACO SPISCES-2B. The simulated transfer characteristics of the proposed poly-Si TFT are shown in Fig.5. The channel length is 10μm and the offset length (L_{off}) is varied from 0.0μm (non-offset) to 1.0μm. The lateral diffusion length which is about 0.2μm is obtained by SUPREM IV. Solid phase crystallized 100nm thick poly-Si film is considered as active layer. Ion impurities injected into the source/drain region are assumed to be activated at 900 ^oC for 30 minutes.

In the proposed TFT, the off current on the negative bias is much less than that of a conventional one. As the L_{off} increases, both the on and off current decrease although the reduction of on current is much less than off current reduction. However, a remarkable suppression in the off current is observed in the offset length of 0.5μm. In order to clarify the major factors dictating the off current, we have evaluated the variation of the peak electric field in the drain depletion region as a function of L_{off}.

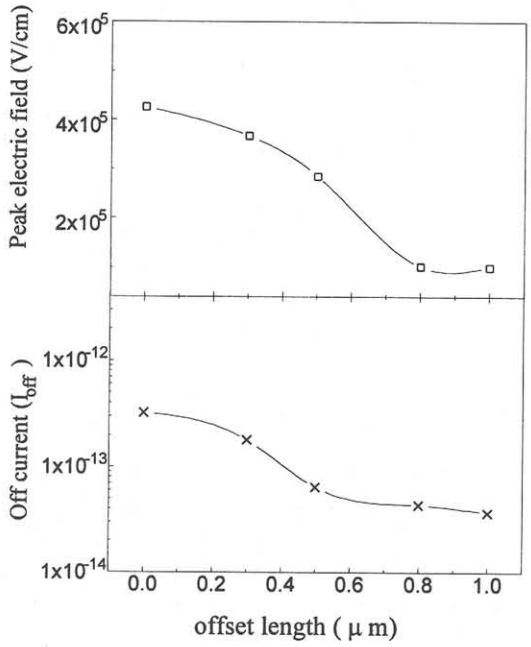

Fig. . 4 Peak electric field strength in the drain depletion region and off current as a function of offset length (L_{off}). V_d= 5V, V_g= -20V

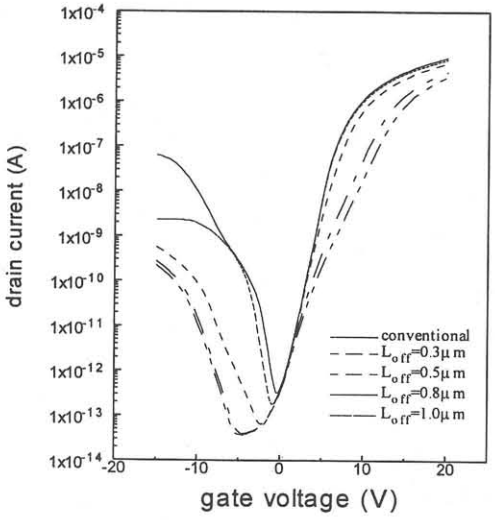

Fig. 5 Transfer characteristics in a conventional and a proposed structure poly-Si TFT. The offset length varies from 0.3μm to 1.0μm. V_d=5V

The peak electric field as shown in Fig.4, decreases with the increase of the offset length. These results imply that the peak electric field is a dominant factor to determine the leakage current. As the offset length increases, the leakage current is reduced from 300 fA to 30 fA. The ON/OFF current ratio with various offset lengths is evaluated as shown in Fig.5. The maximum ON/OFF ratio occurs at L_{off} of 0.5μm and exceeds 10^8.

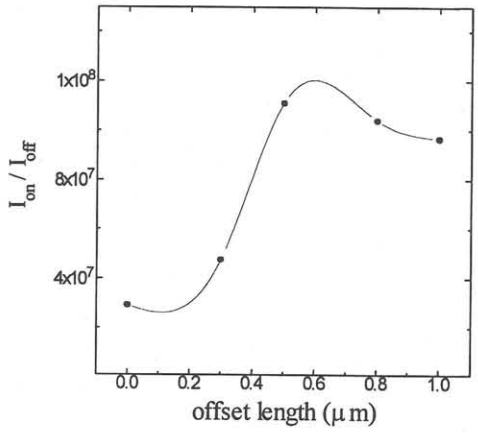

Fig. 6 Variation of on-off current ratio (I_{on}/I_{off}) as a function of offset length (L_{off}).

5. CONCLUSION

We propose a new fabrication process for poly-Si TFTs with a self-aligned offset gated structure by employing a photo resistor reflow process. The offset region by the photo resistor reflow process has been successfully obtained in order to fabricate the offset gated poly-Si TFTs. The symmetrical offset length from 0.5μm to 2.0μm is easily obtained in our experiment. The device simulation shows the maximum ON/OFF ratio of 10^8 at offset length 0.5μm.

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