Effects of GaAs Surface Pretreatment and Post-Growth Annealing on Interface Properties of MBE-ZnSe/GaAs(Sub.) System

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Interface properties of MBE-ZnSeGaAs substrate systems formed on variously pretreated GaAs surfaces including standard chemically etched, (NH₄)₂S₂, NH₄I, HF- and Se-pretreated surfaces, are characterized by C-V and DLTS methods. An HF-pretreated and annealed p-GaAs sample showed marked reduction of interface state density Nₛ, with Nₛ,ₘₕ<4×10¹² cm⁻²eV⁻¹ below the midgap, while C-V curves of n-GaAs samples obtained for the first time indicated the existence of a large Nₛ above the midgap. DLTS method gave consistent results with C-V method. I-Vₓₓ analysis at the interface indicates that Vₓₓ exceeded a few volts for a particular U-shaped distribution.

1. INTRODUCTION

Because of availability of its high quality substrate and close lattice constant with ZnSe, GaAs has been widely used as a substrate for MBE growth of ZnSe and related alloys. By using GaAs substrates, successful operation of ZnSe-based blue/green LDs has been demonstrated by many research groups.² However, degradation of the devices and a low electrical-to-optical conversion efficiency due to a high operation voltage are problems for practical use of the devices. It is clear that ZnSe/GaAs substrate interface is one of keys to improve them, because the interface has a strong effect on the quality of epilayer, some degradation phenomena and electrical properties through its composition and structure. So far, influences of initial growth mode,³ reconstruction during the growth, and substrate preparation method,⁴ on interface state density distribution, Nₛ, have been studied. However, interface properties are still subject of great interest because they are not well understood.

The purpose of the present study is to describe the interface properties of MBE-ZnSe/GaAs substrate systems formed on variously pretreated GaAs surfaces, which include standard chemically etched, (NH₄)₂S₂, NH₄I, HF- and Se-pretreated surfaces, and to describe the effect of post-growth annealing. The influence of interface states on current conduction across the heterointerface is also theoretically analyzed.

2. EXPERIMENTAL

Substrates used in this study were n- and p-GaAs(100) bulk wafers. GaAs was first chemically etched in a 5H₂SO₄:1H₂O₂:1H₂O etchant (a subsequent cleaning in a commercial "semiclean 213" was sometimes employed). Then the substrate was dipped into HF, NH₄I or (NH₄)₂S₂ solutions for 5-10 min. Thermal cleaning of the pretreated surfaces was carried out at 600°C for 5min without As₄ flux. For Se-pretreatment, a thermally cleaned substrate was irradiated by Se-beam flux at a low temperature (<130°C), and then heated to 500°C. Undoped pseudomorphic ZnSe epilayers were grown at 300°C with Se/Zn flux ratio larger than unity. Post-growth annealing was performed in vacuum, H₂ or N₂ ambients at 400°C for 15 min.

Characterization of grown epilayers and interface properties were made by X-Ray Diffraction(XRD), Raman Scattering, C-V and DLTS measurements. For the electrical characterizations, Au/undoped-ZnSe/n- or p-GaAs "pseudo" MIS systems were used.

3. RESULTS AND DISCUSSION

Figure 1 shows RHEED patterns during the growth sequence of ZnSe on a standard chemically etched substrate and on a Se-pretreated substrate. The nucleation of ZnSe occurred at the beginning of the growth, while gradual elongation to a streaky c(2×2) reconstruction pattern was observed thereafter for the chemically etched sample. Much faster elongation to the streaky pattern was observed for HF-pretreated and (NH₄)₂S₂-pretreated samples. A 3-dimensional nucleation in an initial stage of the growth is common feature for Ga-stabilized GaAs substrates. In contrast to those samples, Se-pretreated sample did not indicate the evidence of 3-dimensional nucleation of ZnSe at the beginning of the growth, as seen from Fig.1.
The lattice constant of the ZnSe epilayer was estimated to be 5.684 Å from the angular splitting between ZnSe(400) and GaAs(400) X-ray diffraction peaks. This value is close to the theoretical one for the pseudomorphic ZnSe epilayer on GaAs substrate, i.e. 5.686 Å, calculated from lattice constants of ZnSe and GaAs, and elastic stiffness constants of ZnSe. Figure 2 compares Raman spectra due to LO phonons, for variously pretreated samples. The data were taken at 300K by using an Ar+ laser (4800 Å). Both HF- and (NH4)2S-pretreated samples gave narrower FWHM with enhanced intensity compared with chemically etched sample, indicating quality of epilayers is improved by these pretreatments. Any change in X-ray diffraction curves and Raman spectra was not observed after the post-growth annealing.

Electrical properties of MBE-ZnSe/GaAs interfaces were assessed by C-V and DLTS measurements. For chemically etched p-GaAs samples, measured C-V curves are characterized by a large frequency dispersion of capacitance, a counterclockwise hysteresis, and no accumulation nor inversion of carriers. These characteristics are common to GaAs MIS systems, and interpreted in terms of interface states/2,3. Effects of the pretreatment of GaAs surfaces and the post-growth annealing were clearly reflected in their C-V curves. Figure 3 shows C-V curves of HF-pretreated and annealed Au/MBE-ZnSe/p- and n-GaAs samples. A 1MHz C-V curve in p-GaAs system become steeper by this pretreatment, with less frequency dispersion of capacitance and less hysteresis width, indicating the improvement of the interface properties. Similar improvement was also obtained in (NH4)2S-pretreated p-GaAs sample. Calculated Nm using Terman's method are summarized in Fig.4. HF-pretreated and annealed interface showed marked reduction of interface states with Nm of 4×10^{11} cm^{-2} eV^{-1} below the midgap. The value is about one order of magnitude smaller than that of the standard chemically etched interface, and comparable to reported Nm for (NH4)2S-pretreated interface/3. Since appreciable difference of C-V curves between annealing ambients was not observed and since a Se-pretreated p-GaAs sample gave similar Nm value, as shown in Fig.4, formation of a thin intermediary GaSe/Se-related layer seems responsible for the improvement of the interface properties by the post-growth annealing.

Since non-equilibrium C-V curves are evident in a large positive bias region for p-GaAs samples, owing to large emission time constants of interface states above the midgap, corresponding apparent Nm distributions are indicated by a bold dashed line in Fig.4. Instead, in order to estimate the interface Fermi level position EF above the midgap, C-V curves of MBE-ZnSe/n-GaAs samples were examined for the first time. A considerable lowering of accumulation capacitance with frequency was observed in both HF- and (NH4)2S-pretreated samples, as shown in Fig.3. The result indicates that EF is not completely unpinned due to a high Nm density above the midgap. EF was loosely pinned about 0.5-0.6 eV from the conduction band.
DLTS measurements was performed to confirm the $E_{FS}$ position, since C-V method sometimes misleads the $E_{FS}$ position. Figure 5 shows the resulting Arrhenius plots for the chemically etched samples. Measured bias conditions and the calculated activation energies are indicated in Fig. 5. It is found that DLTS measurements gave consistent results with C-V method in determining $E_{FS}$.

The influence of interface states on current conduction across the interface is theoretically analyzed. Figure 6(a) shows a model of energy-band diagram with U-shaped $N_a$ distribution, under the condition of excess voltage drop $V_{EX}$ across the interface. Here $E_N$ represents a charge neutrality energy level of the interface states, and located at around the minimum point of the U-shaped distribution. When the occupancy of interface states is dominated by imrel of n-GaAs, $I-V_{EX}$ characteristics can be derived from Poisson equation, charge balance equation and energy balance equation based on the thermionic emission theory. Figure 6(b) shows calculated $I-V_{EX}$ characteristics for various $N_a$ distributions shown in the inset. In the calculation, it is assumed that $N_{NP1}=N_{NP2}=1 \times 10^{18}$ $\text{cm}^{-3}$ and $E_C-E_F=1.0$ eV. For U-shaped distributions, experimental $N_a$ distributions are extrapolated within the entire bandgap. A current level of $1 \text{kAcm}^{-2}$, which is estimated from effective Richardson constant for n-GaAs Schottky barrier, is indicated by a horizontal dashed line. It is known that further reduction of $N_a$ density is needed to reduce the operation voltage of LDs or other vertical devices. A comparison with experiment is now undertaken.

4. CONCLUSION

In conclusion, MBE-ZnSe/GaAs substrate systems formed on variously pretreated GaAs surfaces has been characterized. An HF-pretreated p-GaAs sample showed marked reduction of interface state density with $N_{a=\infty}<4 \times 10^{11}$ $\text{cm}^{-2}$eV$^{-1}$ below the midgap after brief annealing. However, C-V curves of n-GaAs samples obtained for the first time indicated that $E_{FS}$ is not completely unpinned due to a high $N_a$ density above the midgap. DLTS measurements gave consistent results with C-V method in determining $E_{FS}$. $I-V_{EX}$ analysis at interface indicates that $V_{EX}$ exceeds a few volts for a particular U-shaped distribution.

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