Numerical Study of Collector-Base Junction Design for Ultra-High-Speed InP/InGaAs Heterojunction Bipolar Transistors

Gregory KHRENOV and Elena KULKOVA[1]

Computer Solid State Physics Laboratory, The University of Aizu, Aizu-Wakamatsu, 965-80, Japan

[1] *Research Center "MICROEL", Krasikov Str. 25a, Moscow, 117218, Russia*

High-frequency operation of non-planar and planar InP/InGaAs HBTs with various collector doping profiles has been investigated using a Monte Carlo particle simulation. It is shown that vertical scaling of collector does not provide a substantial improvement in HBT overall speed performance due to the drastic increase of the collector capacitance charging time with reducing the collector layer thickness. A considerable improvement of HBT high-frequency performance has been obtained in HBT with buried subcollector and non-uniform collector doping profile.

1. INTRODUCTION

In recent years InP/InGaAs heterostructure bipolar transistors (HBTs) have received considerable interest as very attractive candidates for high-speed digital, microwave and long-wavelength fiber-optic communication systems because of the excellent transport property of InGaAs. High-speed InP/InGaAs HBTs having a current gain cutoff frequency about 175 GHz and a maximum oscillation frequency about 167 GHz have been demonstrated in refs.1,2. However, in spite of these incredible microwave characteristics, it does not appear that the InP/InGaAs HBTs are performing up to their potential. It is well-known that the collector capacitance charging time and collector transit time are the main factors which limit the overall speed performance of InP/InGaAs HBTs. Thus, the main problem concerning further extension of HBT frequency range is to reduce these times. The reduction of these times is achieved by using a vertical scaling, realizing a special distribution of the potential in the collector space-charge region to exploit the velocity overshoot effect, and reducing the parasitic elements of transistor structure, in particular the extrinsic base-collector capacitance. In this work the high-frequency performances of InP/InGaAs HBTs with various structures have been thoroughly investigated using a self-consistent Monte Carlo particle simulator to determine how far device performance can be improved by utilizing each techniques.

2. DEVICE STRUCTURES AND MODEL

We have simulated various InP/InGaAs HBTs with an abrupt emitter-base heterojunction. The layouts and cross-sections of simulated HBTs are illustrated in Fig.1. The first HBT is the commonly used HBT with planar subcollector (Fig.1a) and the other one is so-called regrown HBT or HBT with buried subcollector (Fig.1b). Regrown HBT has been recently proposed to reduce the total base-collector capacitance due to the drastic reduction of a large unwanted extrinsic base-collector capacitance.[3] In addition to HBTs with uniformly doped collector layer, we have also investigated the HBTs with non-uniform doping profile of collector layer. The schematic
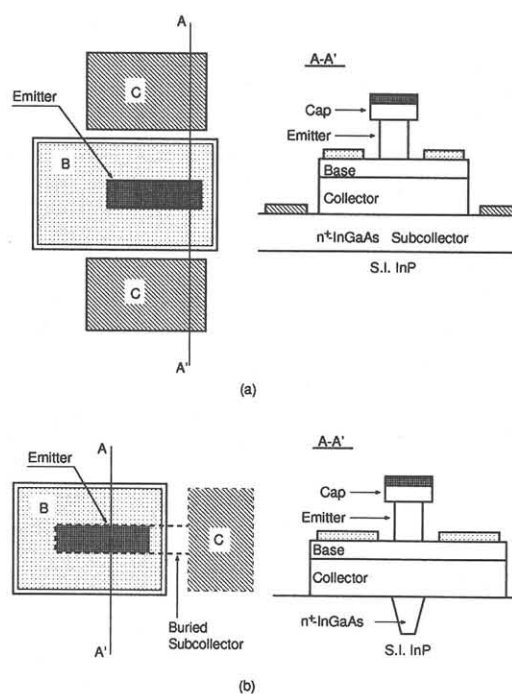

Fig.1 Schematic layouts and cross-sections of (a) conventional HBT with planar subcollector and (b) HBT with buried subcollector.

band diagrams and doping profiles are presented in Fig.2 for HBTs with two different collector layer designs. The proposed non-uniformly doped collector layer is designed to let electrons stay longer in central valley, and hence to keep high electron velocity at least within first half of the collector layer.

Since extreme nonequilibrium electron transport and space-charge effects play an important role in determining HBT high-frequency performance, we have used a self-consistent Monte Carlo particle simulator to study the high-frequency operation of HBT.[4] The ensemble Monte Carlo particle method with a non-parabolic three-valley model is applied to electrons injected from the emitter-base interface. The evolution of the holes in the base layer and electrons in the heavily doped subcollector region is
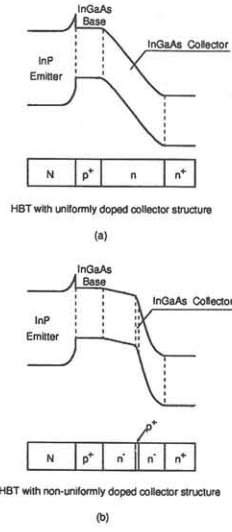
Fig.2 Schematic band diagrams and doping profiles of HBTs with (a) uniformly doped collector and (b) non-uniformly doped collector.

simulated using drift-diffusion approach. The intrinsic base-collector transit delay time is calculated from the Monte Carlo generated impulse response of the induced collector current to a uniformly injected short-time emitter current impulse. The base-collector capacitance is estimated from the steady-state simulation as a ratio of the variation in the total hole charge in the collector-base junction to the corresponding change of the collector-base bias voltage at a fixed collector current.

3. RESULTS AND DISCUSSION

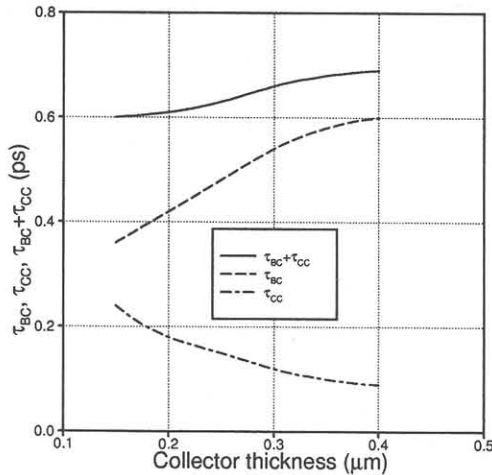First we have investigated a vertical scaling of InP/InGaAs HBT with planar structure. It seems that

Fig.3 Dependencies of the base-collector transit delay time τ_{BC}, collector capacitance charging time τ_{CC} and their sum $\tau_{BC} + \tau_{CC}$ on the collector layer thickness.

continuous reducing the collector layer thickness W_C should lead to improvement of the HBT speed performance because of the reducing transit delay time in collec-

tor space-charge region. However, hand in hand with an decrease in collector transit delay time with reducing W_C is an increase of the base-collector capacitance, and hence an increase of the collector capacitance charging time. Thus, there is a trade-off between these two times. We have simulated a series of HBTs with the similar emitter-base junctions and a range of collector thicknesses from 0.15 to 0.4 μm. Fig.3 shows the collector capacitance charging time τ_{CC}, base-collector transit delay time τ_{BC} and their sum $\tau_{BC} + \tau_{CC}$ versus the thickness of the collector layer. The operation conditions corresponding to full depletion of the collector layer and fixed values of the emitter and collector series resistances have been assumed for this plot. It is seen that the total collector delay time $\tau_{BC} + \tau_{CC}$ drops slightly with reducing W_C because of an essential increase of the collector capacitance charging time in HBTs with very thin collector layers. Moreover, as the collector series resistance R_C increases by a factor 2 the collector charging time becomes the dominant part of the total collector delay time, leading to an increase in $\tau_{BC} + \tau_{CC}$ for HBTs with $W_C \leq 0.2\mu m$ (see Fig.4). Presented results clearly show that drastic reduction of the total delay time is impossible without reduction of the parasitic elements of transistor structure, in particular extrinsic base-collector capacitance.
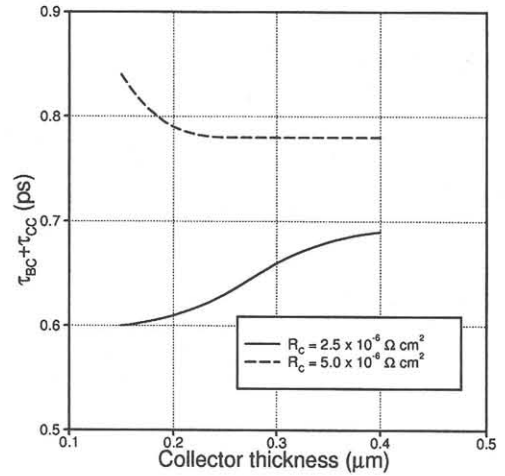

Fig.4 Calculated $\tau_{BC} + \tau_{CC}$ versus the collector layer thickness for two values of the collector series resistance R_C.

An effective solution of this problem is to replace planar subcollector by a buried subcollector (Fig.1b). The HBT with buried subcollector is expected to have very small extrinsic base-collector capacitance due to the small overlap area between subcollector region and base layer. We have calculated the base-collector capacitances of HBTs with planar subcollector and HBTs with buried subcollector. The total base-collector capacitances C_{CT} versus collector-base voltage are demonstrated in Fig.5 for both considered HBT designs. The normalization factor C_0 corresponds to the total base-collector capacitance of the planar HBT with fully depleted collector n-layer. Analysis shows that the collector capacitance of regrown HBT

with uniformly doped collector layer (solid curve) is extremely small under the high voltages, and is practically equal to the capacitance of planar HBT (dashed curve) under the low voltages. This unexpected fact results from the distributed two-dimensional nature of the collector capacitance of regrown HBT. Under the relatively low applied voltages V_{CB} <1.5 V the collector n-layer is not fully depleted. As a result, the base-collector capacitance is determined by the thickness of the depletion collector region and coincides with corresponding capacitance of planar HBT. In contrast, under the high applied voltages V_{CB} >2.25 V the collector layer is fully depleted and base-collector capacitance of regrown HBT is determined as a geometrical capacitance between high conductive base layer and subcollector region. Thus, the implementation of buried subcollector leads to drastic reduction of the collector capacitance charging time only under the high applied collector voltages. However, the minimum collector transit time is observed under the low collector-base voltages.[5,6] To overcome this contradiction we have proposed and simulated InP/InGaAs HBTs with non-uniform collector doping profile. The standard collector n-layer has been replaced by a very thin p^+ layer inserted between two lightly doped n^- layers (see Fig.2). Proposed design provides small value of the total base-collector capacitance down to very low applied voltages (dot-dashed curve in Fig.5) and has an important side benefit. The distribution of the electric field corresponding to this doping profile is very favorable to exploit overshoot effect in the collector space-charge region, resulting in considerable reduction of the collector transit time.
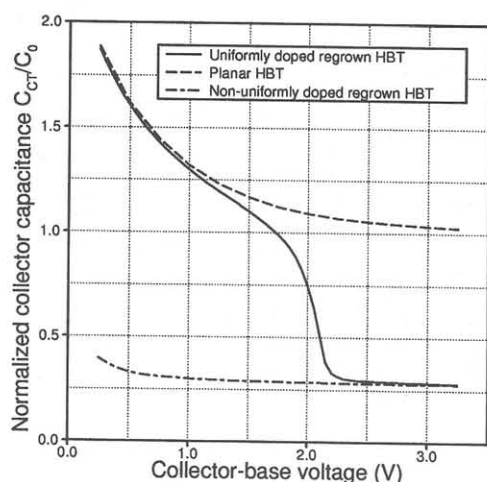

Fig.5 Normalized collector capacitance versus collector-base voltage for HBTs with various collector structures.

The electron transport in the base-collector junctions of HBTs with $W_C = 0.3\mu m$ and two different collector doping profiles has been simulated at 300 K. The emitter-base junctions are the same for both considered HBTs. The collector n-layer of standard HBT is doped at 2×10^{16} cm^{-3}, and proposed HBT has non-uniformly doped collector consisting of very thin 20-Å p^+ $(1 \times 10^{18}$ cm$^{-3})$ layer inserted between two 1500-Å lightly

doped n^- $(3 \times 10^{15}$ cm$^{-3})$ layers. The collector current density 10^5 A/cm^2 is assumed throughout this simulation. The base-collector transit delay times τ_{BC} as functions of the collector bias are presented in Fig.6 for HBTs with uniform and non-uniform collector doping profiles. It has been found that in the wide range of applied voltages the improvement rate in τ_{BC} by utilizing non-uniform doping profile is approximately 30% compared with uniformly doped HBT.
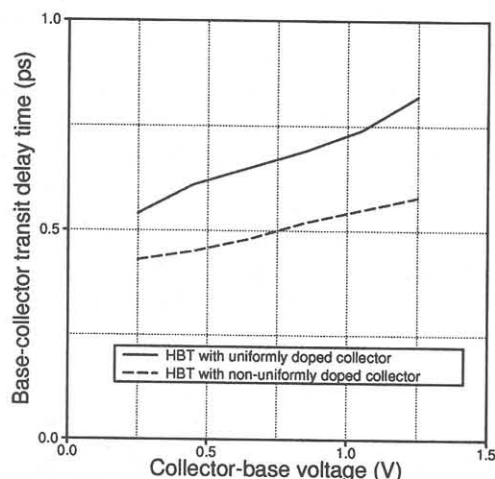

Fig.6 Dependencies of the base-collector transit delay time on the collector-base voltage for HBTs with various collector doping profiles.

4. CONCLUSIONS

The InP/InGaAs HBTs with various structures have been investigated using an ensemble Monte Carlo simulation to understand how HBT high-frequency performance can be improved by using a vertical scaling, exploiting a near-ballistic transport and implementing a special design of subcollector region. Results of numerical simulation show that the vertical scaling of collector layer alone does not result in a considerable improvement in overall speed performance of HBT. The most attractive way to enhance overall speed performance of InP/InGaAs HBT is to exploit velocity overshoot effect in HBT with buried subcollector.

References

1) J-I.Song, B.W-P.Hong, C.J.Palmstrom, B.P.Van der Gaag and K.B.Chough: IEEE Electron Device Lett. **15** (1994) 94.

2) H.Shigematsu, T.Iwai, Y.Matsumiya, H.Ohnishi, O.Ueda and T.Fujii: IEEE Electron Device Lett. **16** (1995) 55.

3) J-I.Song, M.R.Frei, J.R.Hayes, R.Bhat and H.M.Cox: IEEE Electron Device Lett. **15**(1994) 123.

4) G.Khrenov, V.Ryzhii and S.Kartashov: Proc. 2nd Int. Conf. VLSI and CAD, 1991, Seoul, p.215.

5) R.N.Nottenburg, Y.K.Chen, M.B.Panish, D.A.Humphrey and R.Hamm: IEEE Electron Dev. Lett. **10** (1989) 30.

6) A.F.J.Levi, R.N.Nottenburg, Y.K.Chen, P.H.Beton and M.B.Panish: Solid-State Electron. **32** (1989) 1289.