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Excellent Thermally-Stable Epitaxial Channel for Implanted Planar-Type Hetero-Junction Field-Effect Transistors

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We demonstrate for the first time that highly doped thin GaAs epitaxial layers are thermally stable. Thermally-stable channels are applied to implanted planar-type two-mode channel field-effect transistors. A 0.2 μm device having a GaAs channel of 9 nm thickness with a doping level of $7x10^{18}$ cm^{-3} exhibits excellent performance, such as a transconductance *gm* of 450 mS/mm, a current-gain cutoff frequency *fT* of 72 GHz, and a maximum frequency of oscillation *fmax* of 140 GHz. It is also suggested from the excellent performance that such thin layers have another merit of difficulty in thermally diffusing dopants.

1. Introduction

Hetero-junction field-effect transistors (FETs) using III-V compound semiconductors, such as high electron mobility transistors (HEMTs) and two-mode channel FETs (TMTs), have been widely studied for microwave/millimeter-wave systems, e.g., direct satellite broadcasting communication systems and vehicle collision avoidance systems, because of their excellent low-noise, high-power performance, and high-frequency operation. The planar-type structure of these devices is very suitable for achieving good uniformity and reproducibility of the device characteristics necessary for MMICs and MIMICs. In order to realize planar-type devices, an ion implantation technique including a post-implantation annealing process is necessary for the formation of source and drain n^+ regions. However, there are two serious problems for the fabrication of implanted hetero-junction FETs; that is, the decrease of carrier concentration and the impurity-diffusion in their doped layers by annealing. In particular, these phenomena appear at highly doped layers. For example, this kind of annealing-induced carrier concentration decrease appears often in highly doped GaAs layers.[1] Also, impurity-diffusion can be seen in annealing selectively doped GaAs/n-AlGaAs heterostructures, and is enhanced with an increase of the doping level in n-AlGaAs.[2] On the other hand, however, employing highly doped active layers has recently received much attention for attaining high performance in hetero-junction FETs. [3]

In order to resolve these difficulties, we experimented and found new evidence that thinning GaAs epitaxial layers is a very effective way to minimize the annealing-induced carrier concentration decrease even at high doping levels. In this article, we describe the thermal stability of highly doped GaAs layers and their application to planar-type TMTs (P-TMTs).[4]

2. The effects of annealing on doped GaAs layers

First of all, the effects of rapid thermal annealing on GaAs layers with various doping conditions were investigated. Samples grown by molecular beam epitaxy (MBE) on undoped (100) GaAs LEC substrates included three Si doping levels of $2.5x10^{18}$ cm^{-3}, $5x10^{18}$ cm^{-3}, and $7.5x10^{18}$ cm^{-3}. The thickness of the doped layers was varied in the range of 10-50 nm, which is frequently used for practical device structures. The wafers were encapsulated by SiN double-layered films deposited by electron-cyclotron-resonance plasma chemical vapor deposition (ECR-PCVD), followed by annealing at 880 °C for 5 s. The carrier concentration of the doped GaAs layers before and after annealing was determined by Hall-effect and capacitance-voltage measurements. Figure 1 shows the decrease in carrier concentration by annealing as a function of the thickness of the doped layers. As can be seen in the figure, it is found that the decrease in carrier concentration becomes severe with increases in the doping level. This is consistent with

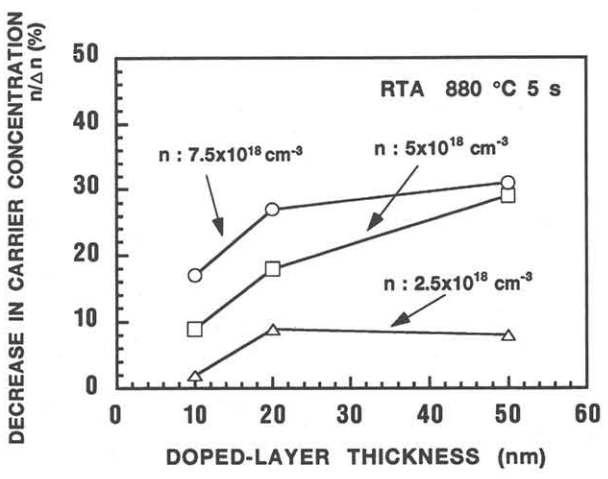

Fig. 1. Decrease in carrier concentration by annealing as a function of the thickness of the doped layers

the results obtained by annealing GaAs/n-AlGaAs heterostructures.[2] However, it is very interesting to note that by thinning the doped layers the degree of the decrease becomes less at every doping level. Even at heavily doped layers with $7.5x10^{18}$ cm^{-3}, the degree can be reduced from 30% to 17% by thinning the layers from 50 nm to 10 nm. This indicates that thinning the doped layers can make them more thermally stable.

The annealing-induced carrier concentration decrease has been explained in connection with self-activated (SA) centers, which are complexes comprising a donor atom and Ga vacancy (V_{Ga}).[5] It has been also presented that the degree of the decrease increases with SA centers.[1] Since we also observed similar results, the decrease is possibly due to the generation of V_{Ga} acceptors and related SA centers. Here, there is a most important question as to why the annealing-induced carrier concentration decrease becomes less by thinning the doped GaAs layer. Before considering the reason, we briefly refer to the formation mechanism of V_{Ga} in GaAs. Walukiewicz claimed that the formation energy of an ionized V_{Ga} decreases with an increase in the Fermi energy.[6] This means that the concentration of V_{Ga} increases with Fermi energy. So, the elevation of the Fermi energy by higher n-type doping causes a higher density of V_{Ga}, and hence a higher density of SA centers. Thus, the annealing-induced carrier concentration decrease is thought to become severe with an increase in the doping level. Also, for doped thin layers such as those used in this experiment, the electron distributions are a 2-dimensional-like configuration. In the case of a 2-dimensional electron gas configuration, a lower sheet carrier concentration causes a lower Fermi energy.[7] Thus, we believe that thinning a doped layer causes lowering of the Fermi energy in the region of the doped layer, thereby suppressing the generation of V_{Ga}, and hence the annealing-induced carrier concentration decrease.

3. Device structure and fabrication procedure

We applied thermally-stable, highly doped GaAs channels to P-TMTs. Figure 2 shows a schematic diagram of the device structure. The wafer consists of an undoped GaAs buffer layer (800 nm), an undoped $In_{0.2}Ga_{0.8}As$ channel layer (5 nm), an undoped graded $In_xGa_{1-x}As$ channel layer (In mole fraction 0.2 (lower side)~0 (upper side); 7 nm), an undoped GaAs spacer layer (5 nm), an n-GaAs electron-supplying and channel layer, and an undoped GaAs barrier layer. Here, P-TMT structures with the following two Si-doped GaAs channels have been investigated: one is 9 nm-thick with a doping level of $7x10^{18}$ cm^{-3}, the other is 20 nm-thick with a doping level of $3x10^{18}$ cm^{-3}. The degree of the annealing-induced carrier concentration decrease was designed to be as small as 12-15%. Also, to unify the distance from the surface to each center of the doped channels for the sake of simplifying the comparison, the thickness of the undoped barrier layers was designed to be 25.5 nm and 20 nm for the wafers with $7x10^{18}$ cm^{-3} and $3x10^{18}$ cm^{-3} doped channels, respectively. Each sample was grown by MBE at a growth temperature of 500 °C.

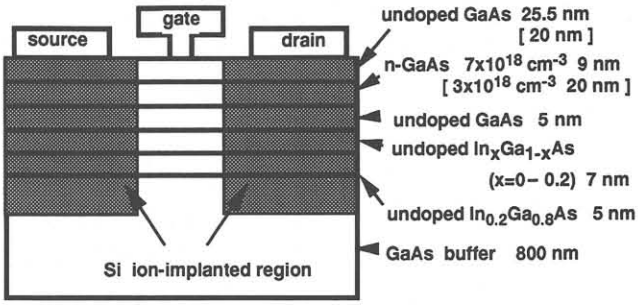

Fig. 2 . Schematic cross section of planar-type TMT structure

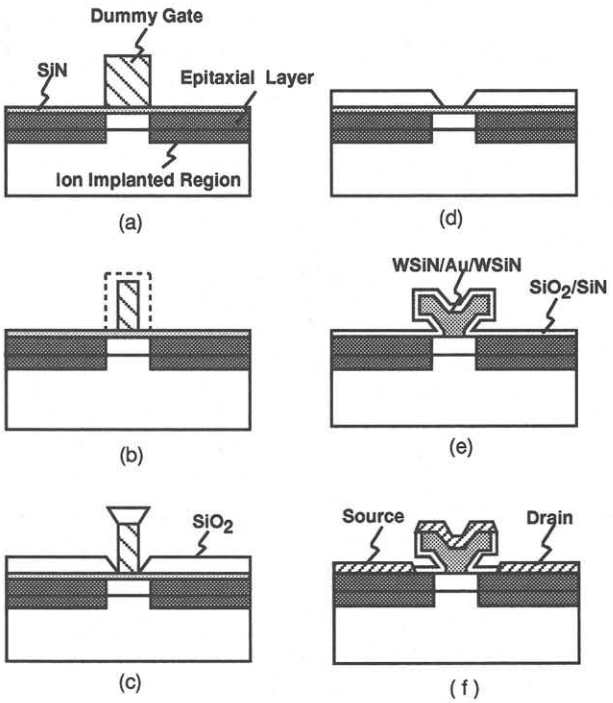

Fig. 3 . Device fabrication process of P-TMT

The device fabrication process for our advanced n^+ self-aligned P-TMT is shown in Fig. 3. After device isolation through mesa etching, an ECR-PCVD SiN double-layered film was deposited for an annealing cap. The film properties of this annealing cap were optimized to achieve high activation of the implanted ions. Next, a 0.6 μm-length dummy-gate pattern was shaped using a PMMA photoresist. To form self-aligned n^+ regions, a high dose ($5x10^{13}$ cm^{-2}) Si implantation at 90 keV was carried out with the dummy-gate pattern as an implantation mask (Fig. 3(a)). The dummy-gate pattern was thinned from 0.6 μm to 0.2 μm by an oxygen plasma process (Fig. 3(b)). After ECR-PCVD SiO_2 deposition followed by selective wet etching

(buffered HF) of the SiO_2 deposited on the sidewall of the dummy-gate resist (Fig. 3(c)), the reverse dummy-gate pattern was formed by removal of the resist, followed by rapid thermal annealing at 880 °C for 5 s (Fig. 3(d)). A T-shaped WSiN/Au/WSiN gate electrode was formed by sputtering and ion-milling techniques. Here, the SiN/SiO_2 film was removed to reduce the parasitic capacitance under the T-shaped gate, and then a SiO_2/SiN encapsulant was newly deposited, followed by annealing at 450 °C to minimize sputtering-damage (Fig. 3(e)). Finally, alloyed AuGe/Ni/Au metal was formed for the source and drain ohmic contacts. Here, the T-shaped gate served as a shadow mask during the deposition, allowing the ohmic contacts to be self-aligned to the gate (Fig. 3(f)).

4. Device characteristics

For the 0.25x100 μm gate P-TMTs with $7x10^{18}$ cm^{-3} and $3x10^{18}$ cm^{-3} doped GaAs channels, the extrinsic transconductance and drain current as a function of the gate voltage, and the current gain $|H_{21}|$ and unilateral gain U as a function of frequency are shown in Fig. 4 and Fig. 5, respectively. As shown in these figures, the $7x10^{18}$ cm^{-3} sample exhibits excellent performance, such as a *gm* of 450 mS/mm, an f_T of 72 GHz and an f_{max} of 140 GHz, compared with the $3x10^{18}$ cm^{-3} sample which has a *gm* of 350 mS/mm, an f_T of 62 GHz and an f_{max} of 122 GHz. The results indicate that highly doped thin layers are very effective for improving DC and microwave performance in the case of P-TMTs as well as in the case of recessed-gate hetero-junction FETs with no high-temperature treatment.[3] This advantage is supported by suppressing the annealing-induced carrier concentration decrease despite the extremely high doping level of $7x10^{18}$ cm^{-3}. Furthermore, taking into account the lack of annealing-induced degradation in device performance, such as good pinch-off characteristics of the subthreshould region shown in Fig. 4, Si-diffusion from the doped GaAs layer to the undoped InGaAs well during the annealing is thought to be negligible and, accordingly, its length is inferred to be less than 5 nm. This is surprising because the diffusion-length is far shorter than the expected value from the reported Si-diffusion rate.[8] Thus such thin layers have another merit of difficulty in thermally diffusing dopants.

5. Conclusions

We experimentally demonstrated for the first time that highly doped thin GaAs epitaxial layers are thermally stable. Based on this evidence, thermally-stable channels were applied to implanted P-TMTs. The 0.2 μm device having a GaAs channel of 9 nm thickness with a doping level of $7x10^{18}$ cm^{-3} exhibits excellent performance, such as a *gm* of 450 mS/mm, an f_T of 72 GHz, and an f_{max} of 140 GHz. It was also suggested from the excellent performance that such thin layers have a merit of difficulty in thermally diffusing dopants. Therefore, our findings are also applicable to other planar-type hetero-junction FETs, such as HEMTs and doped-channel FETs.

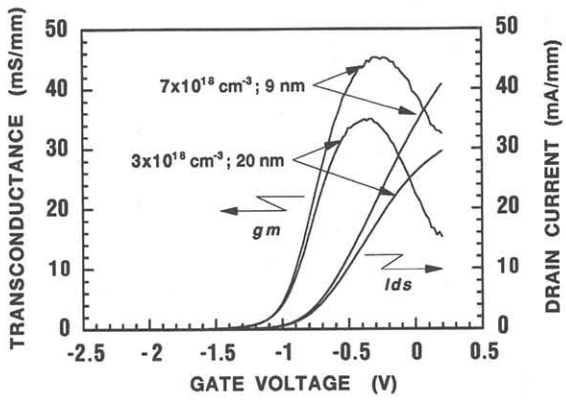

Fig. 4. Transconductance and drain current as a function of gate voltage for two types of P-TMTs

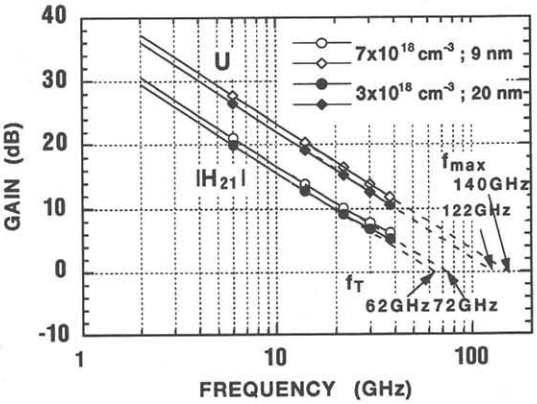

Fig. 5. Current and unilateral gain as a function of frequency for two types of P-TMTs

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