Fabrication of Quantum Wire and Minute Buried Heterostructure by In-Situ Etching and Selective MOCVD Growth

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Abstract

Among the various methods used for the fabrication of III-V semiconductor quantum nanostructures:

1. Flow rate modulation epitaxy (FME) on a patterned substrate, 2. In-situ dry-etching and regrowth process, and 3. In-situ gas-etching and regrowth process; are presently investigated from the view points of interface quality, uniformity, and freedom in the structural and material design.

1. FME growth on a patterned substrate

Flow rate modulation epitaxy (FME) has been initially developed to decrease the growth temperature of GaAs by supplying arsine and gallium alternatively. 1) This technique is also applicable to realize an AlGaAs/GaAs quantum wire with strong lateral confinement. Figure 1 shows a cross-sectional transmission electron microscopy (TEM) picture of stacked quantum wires prepared by FME on a V grooved substrate at Crescent shaped GaAs quantum wires with a 630°C.²⁾ vertical width of 9nm and a lateral width of 28 nm have been embedded in AlGaAs. Growth of GaAs along the (111)A side wall is almost suppressed by the enhanced surface migration of gallium atoms at arsenic lean periods of the FME. Al_{0.3} Ga_{0.7} As layers were grown by a conventional MOCVD technique. Sizes and separation of quantum wires have been adjusted simply by the growth time of GaAs and AlGaAs Therefore, coupled quantum wires with adjustable coupling intensity have been realized.3) Low growth temperature is effective to reduce the impurity incorporation into the epitaxial layer and resulted in a narrow 7 meV line width of the photoluminescence (PL) spectra. The PL line width above 200K is narrower than that of a conventional quantum well as is seen in Fig.2, therefore, theoretical advantage of quantum wire over quantum well, which has been hidden behind the structural inhomogeneity, is verified.

2. In-situ electron cyclotron resonance (ECR) dryetching and regrowth process

The dry etching technique has the largest freedom in the layout design because it has no dependence on the crystalline plane. Fig.3 shows the schematic design of an MOCVD furnace equipped with an ECR dry etcher together with an explanation of the processing steps. A quantum well (QW) wafer patterned with SiO₂ (or tungsten) film is introduced to the ECR etcher through load lock chamber and etched to a depth of 2.8 µm. We found that an inorganic mask, such as SiO2, is usable for dry etching and subcequent selective regrowth to form a buried heterostructure.4) Figure 4 shows a scanning electron microscopy (SEM) cross-section of a small heterostructure. The side wall of a graded index separate confinement heterostructure is embedded with regrown AlGaAs and an active region width of 0.5 µm is defined. High aspect ratio of around 5 is obtained. The spectra linewidth and normalized intensity of the PL to the stripe width are similar to those recorded from the starting planar quantum well at cooled temperature. However, TEM observation reveals high dislocation density at the regrown interfaces which causes a surface recombination velocity of the order of 103 m/s at room temperature. This limits the practical application of this technique to a relatively large structure such as semiconductor laser and opto-electronic integrated circuits (OEICs).

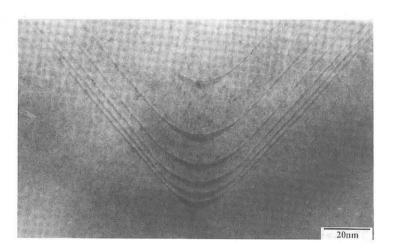


Fig 1. Cross-sectional TEM picture of a quantum wire prepared by FME on a V grooved substrate at 630°C.

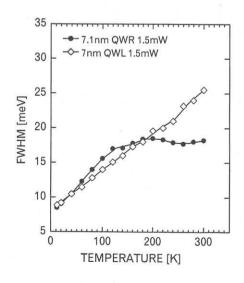


Fig.2 Temperature dependence of PL line width for a quantum wire and a quantum well .

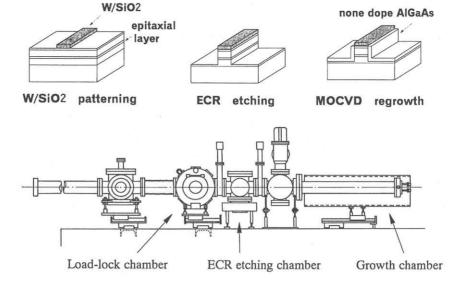


Fig.3 schematic design of an MOCVD furnace equipped with an ECR dry etcher together with an explanation of the processing steps.

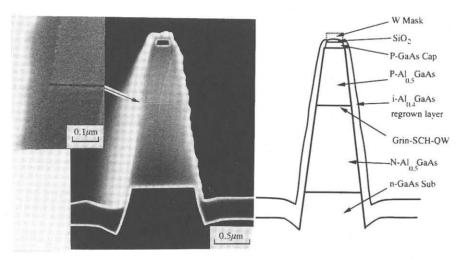


Fig. 4 SEM cross-section of a small buried heterostructure prepared by in-situ dry-etching and regrowth.

3. In-situ gas-phase etching and regrowth process

In order to improve the interface quality, an in-situ gas-phase etching and regrowth process has been investigated using ${\rm SiO_2}$ as a selective mask. The advantages of the in-situ gas-phase etching over dry-etching are: firstly, there is no damage by ion bombardment; secondly, etching is performed in the same growth furnace without interruption for sample transfer.

Figure 5 shows the InGaAs/GaAs multi-quantum well by HCl gas-phase etching at 730°C together with a small amount of TEGa and arsine, and immediate regrowth of AlGaAs. A perpendicular side-wall of (011) plane is clearly revealed along the [011] direction of SiO₂ mask. The TEGa and arsine help to make the etching process close to the thermal equilibriumt condition.⁵⁾ A (111)A side-wall plane appears along [0-11] direction. Etch rate of AlGaAs is very small with HCl gasphase etching. This technique is limited only to GaAs and InGaAs layers without aluminium.

Chlorine is known to have similar etching velocity for both GaAs and AlGaAs. However, it is used with nitrogen or high vacuum at relatively low temperature.⁶) Alkyl-chloride is more

suitable for in-situ gas-phase etching of AlGaAs because it can be used in hydrogen atmosphere at growth temperature of 600 $\sim 700\,^\circ\text{C}$. Figure 6 shows the SEM cross-section of a quantum wire prepared by in-situ $C_2H_5\text{Cl}$ gas-phase etching, with a small amount of arsine, and regrowth technique. The quantum well with a thickness of 8 nm is etched from both sides of the SiO2 mask to a depth of 60nm and the side walls are embedded with the regrown AlGaAs, resulting in a quantum wire width of 30 nm. The initial width of electron-beam resist (SAL601) was 60 nm. Therefore, wire width narrower than lithographic limitation is obtained by the lateral etching of SiO2 with buffered hydrofluoric acid and AlGaAs with $C_2H_5\text{Cl}$ gas.

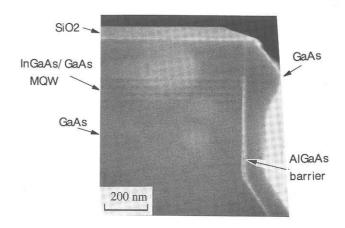


Fig.5 SEM cross-section of GaAs/InGaAs QW and AlGaAs barrier layer prepared by in-situ HCl gas-etching and regrowth.

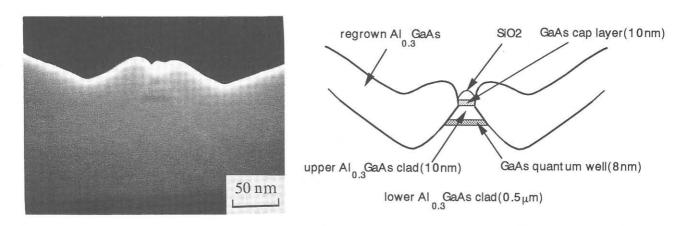


Fig.6 SEM cross-section of AlGaAs/GaAs quantum wire prepared by in-situ alkyl chloride gas-etching and regrowth.

4. Conclusion

In conclusion, one time growth on a patterned substrate realizes the best interface quality and uniformity. For the first time, the PL line width of quantum wires near room temperature is narrower than that of the quantum well. This open the possibility of improved performance of practical devices in the quantum wire structure.

The advantage of etching and regrowth processes is the freedom in the layout design. In the case of dry-ething we are able to form a buried heterostructure exactly as we pattern the inorganic mask without any consideration for the crystal orientation. To start from the well defined (100) plane is another merit because doping behavior is difficult on a (111)A plane in the V grooved substrate. However, growth interface has a lot of defects and it invoked the study of additional gas-phase etching.

Gas-phase etching is very attractive because the instrumentation is simpler than for dry etching and lithographic design of the structure is still possible. We demonstrated that very smooth surface morphology can be obtained at a certain condition near thermal equilibrium, though etched depth profile is affected by the pattern size and is not fully controlled yet.

Any way, combination of the aforementioned techniques will improve the freedom of the structural design for 3 dimensional nanostructure devices.

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References

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- 1) N.Kobayashi, T.Makimoto, and Y.Horikoshi, Jpn.J.Appl.Phys. **24**, (1985) L962.
- 2) Xue-Lun Wang, Mutsuo Ogura, and Hirofumi Matsuhata, Appl.Phys. Lett **66** (1995) 1506.
- 3) K.Komori, X.L.Wang, M.Ogura, and H.Matsuhata, to be presented at the 22th int. symp. on compound Semiconductors.
- 4) M.Ogura, J.Vac. Sci. Technol. B 13(4), (1995) in press. 5) Xue-Lun Wang and M.Ogura, Proc. of 13th compound semiconductor electronics symposium, F-12 (1994)
- 6) H.Kawanishi, Y.Sugimoto, K.Akita, N.Tanaka and T.Ishikawa, Appl. Phys.Lett. **60**, (1992) 365.