Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 977-979

The Capacitance of Nano-Structures

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ABSTRACT

The nano-structure capacitance is analyzed and is shown to consist of three components serially connected; one is the extension of the classical capacitance in electrostatics, another is due to the electronic density of states of the conductor, and the other comes from the electronic charge distribution inside the conductor. The latter two have only the self-capacitance contribution. The diagrammatic expression of the capacitance is given. As an example, the C-V curve of dual gate SOI MOS junction is evaluated.

1. INTRODUCTION

According to technology trends widely accepted, it is highly probable that the feature size of micro-devices and circuits will leap into the sub-tenth micrometer range at the beginning of next century. There, the general feature of capacitance is supposed to undergo a serious modification compared with that of the larger size structure, just as the conductance of the nano-structure are subjected to a remarkable change due to the quantum mechanical effect. The capacitance of microstructures is discussed by some authors[1),2)] and the contribution from the electronic density of states has been pointed out. It is important to enumerate all contributions of nano-structure capacitance and discuss them from the general point of view. This paper has discussed the general expression of the nano-structure capacitance with use of the one-electron picture based on the self-consistent field approximation, and has shown the presence of extra-components due the micro-size effect in addition to the classical electrostatic capacitance. In the analysis of single electron devices especially, the capacitance plays a key role and the consideration of these detailed nano-structure capacitance will become increasingly important as the device size is scaled down.

2. EXPRESSION OF CAPACITANCE

We assume a system that consists of a number of micro-size bodies of conductors (metals and semiconductors) separated by insulator region from each other, as is exemplified in Fig.1. The charge on the i-th conductor Q_i is not a simple function of the electrode potentials of the j-th conductor ϕ_j's generally, and we need to define the capacitance matrix element $\hat{C}_{ij}$ with use of the differential expression, $\delta Q_i = \sum_j \hat{C}_{ij}\delta\phi_j$.

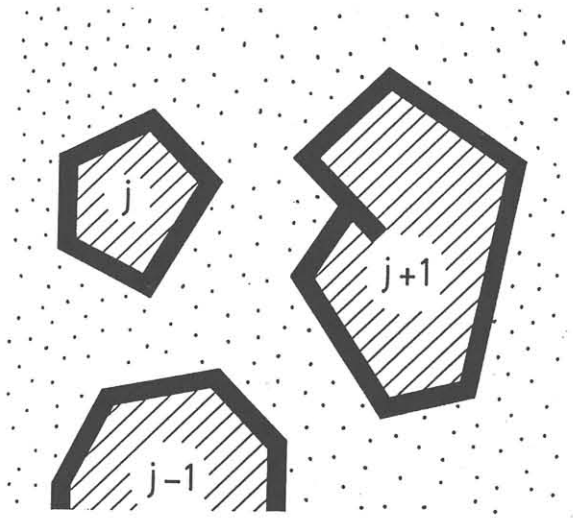

Fig.1. A nano-structure where conductors are set separated by insulator region.

Since the ionic charge on the conductor is fixed, the charge increment Q_j can be substituted for the increment of the electronic charge on the conductor, and is expressed in the one-electron picture as

$$\delta Q_j = \delta((-e)\int D_j(E, Q_j, V_j(\mathrm{s}))f(\mu_j, E)dE). \quad (1)$$

Here $D_j(E, Q_j, V_j(\mathrm{s}))$ is the electronic density of states of the j-th conductor and is the function of the energy E, the charge Q_j, and the electric potential on the surface point s of the conductor, $V_j(\mathrm{s})$, which is the function of Q_j and Q_i's ($i \neq j$). e is the electronic charge, and $f(\mu_j, E)$ is the Fermi distribution function with the Fermi potential μ_j. The electrode potential of the j-th conductor means the necessary energy for unit charge addition to the conductor and corresponds to the chemical potential of the conductor, which is well approximated by the Fermi potential μ_j in our case, i.e. $\phi_j = \mu_j/(-e)$.
A straight-forward evaluation will lead us to the expression of the capacitance matrix $\hat{C}$,

$$\hat{C}^{-1} = \hat{C}_D^{-1} + \hat{C}_Q^{-1} + \hat{C}_C^{-1} \quad (2)$$

where the matrices $\hat{C}_D$, $\hat{C}_Q$ and $\hat{C}_C$ are defined by expressions,

$$(\hat{C}_D)_{ji} \equiv (-e)^2 \int D_j(E, Q_j, V_j(\mathbf{s})) \frac{\partial f(\mu_j, E)}{\partial \mu_j} dE \delta_{ji} \quad (3)$$

$$(\hat{C}_Q)_{ji} \equiv \frac{e \int D_j(E, Q_j, V_j(\mathbf{s})) \frac{\partial f(\mu_j, E)}{\partial \mu_j} dE}{\int \frac{\partial D_j(E, Q_j, V_j(\mathbf{s}))}{\partial Q_j} f(\mu_j, E) dE} \delta_{ji} \quad (4)$$

$$(\hat{C}_C^{-1})_{ji} \equiv \frac{\int \int \frac{\delta D_j(E, Q_j, V_j(\mathbf{s}))}{\delta V_j(\mathbf{s})} \frac{\partial V_j(\mathbf{s})}{\partial Q_i} ds f(\mu_j, E) dE}{e \int D_j(E, Q_j, V_j(\mathbf{s})) \frac{\partial f(\mu_j, E)}{\partial \mu_j} dE}, \quad (5)$$

where $\delta D/\delta V$ denotes the functional derivative. These expressions are complex and their physical images are not clear. However, we can easily derive approximate expressions of these quantities which suggest more clearly what these quantities mean.

The $(\hat{C}_C^{-1})_{ji}$ is further transformed to

$$(\hat{C}_C^{-1})_{ji} \approx \frac{\partial V_{j0}}{\partial Q_i}, \quad (6)$$

where $V_{j0} \equiv \int V_j(\mathbf{s}) ds / \int ds$ is the average value of electric potential over the surface of the j-th conductor. Eq.(6) suggests that this quantity coincides with the classical capacitance for the perfect conductor system, and we can see that $\hat{C}_C$ means the extended concept of the classical capacitance due to insulation.

At low temperatures where carriers are degenerate, we obtain

$$(\hat{C}_D)_{ji} \approx e^2 D_j(\mu_j, Q_j, V_j(\mathbf{s})) \delta_{ji}, \quad (7)$$

i.e. this component is diagonal and it gives the electronic density of states at the Fermi potential. At the room temperature, it is evaluated as

$$(\hat{C}_D)_{ji} = \frac{e}{kT} |q_j| \delta_{ji}, \quad (8)$$

where q_j is the electronic charge in the j-th conductor. The expression of $\hat{C}_Q$ also is transformed to

$$(\hat{C}_Q)_{ji} \approx \left[-\frac{\partial E_{\ell j}(Q_j, V_j(\mathbf{s}))}{e \partial Q_j} \right]^{-1}_{E_{\ell j}(Q_j, V_j(\mathbf{s})) \approx \mu_j} \delta_{ji}. \quad (9)$$

at low temperatures, where $E_{\ell j}(Q_j, V_j(\mathbf{s}))$ denotes the ℓ-th energy level of the conductor. Eq.(9) gives the variation of the energy level which is measured from V_{j0} and coincides with the Fermi potential, when the charge on the conductor is varied. This component is due to the charge delocalization off the surface into the bulk of conductor. For example of MOS inversion layers, the $\hat{C}_C$ component provides the normal MOS capacitance due to the oxide insulation, while $\hat{C}_Q$ component gives the capacitance contribution due to the fact that the center of mass of inversion charge is separated from the interface toward inside.

When the capacitance is composed of two-body capacitance components, it is convenient to use a diagrammatic expression. Suppose that the classical capacitance network is expressed with two-body capacitance components as is shown in Fig.2(a). Then the counterpart for nano-structure capacitance taking account of the quantum mechanical effect is expressed with the diagram shown in Fig.2(b). Of course $C_C(j,i)$, $C_Q(j)$ and $C_D(j)$ are those quantities evaluated with Eqs.(3),(4) and (5), and do not coincide with the classical value generally. The charge on hypothetical nodes j', j'' etc. should be put to zero in the calculation.

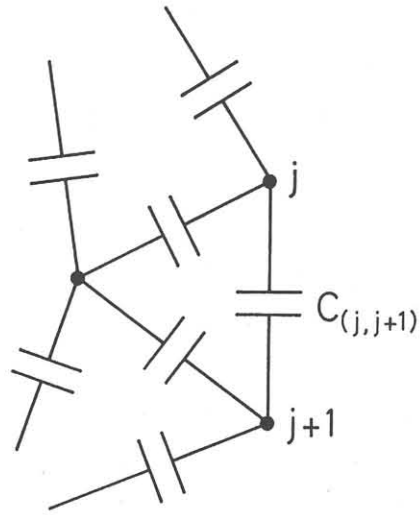

Fig.2(a). Classical capacitance network.

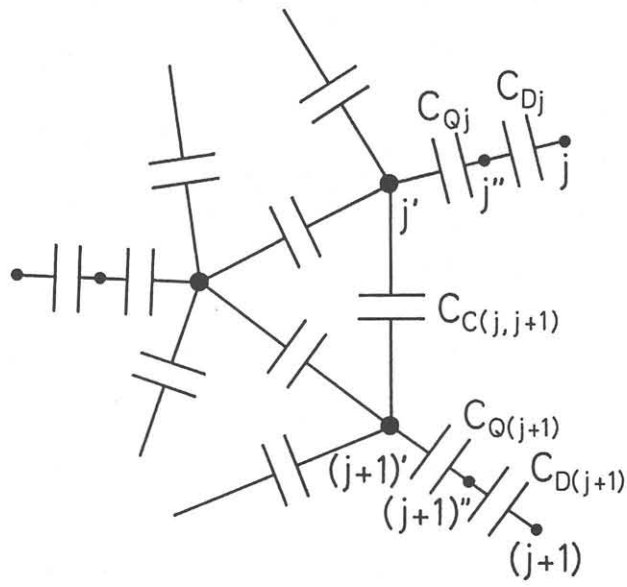

Fig.2(b). Nano-structure capacitance network corresponding to Fig.2(a).

3. DUAL GATE SOI MOS JUNCTION

As an example of the nano-structure capacitance, the

C-V curve of the dual gate SOI MOS junction was computed. The device structure analysed is shown in Fig.3, where Gate1 and Gate2 are arranged in a symmetrical position and the same gate bias voltage is applied. The C-V curve was computed with the Hartree approximation, self-consistently solving the Schrödinger equation and the Poisson equation. The computed C-V curve for 5 nm SOI thickness at 10 K and 300 K are shown in Fig.3. The SOI channel is assumed of intrinsic Si. The characteristic staircase-like structure shown at low temperature is due to the $\hat{C}_D$ component of capacitance and reflects the two-dimensional electronic density of states. The staircase-like structure appears every time the Fermi potential jumps into the new sub-band and the density of states there steps up. At the room temperature, this component reflects the quantity of electronic charge in the conductor and shows smooth increase as the gate bias is increased as is shown in the figure. The variation of $\hat{C}_Q$ component is gentle and produces no conspicuous structures.

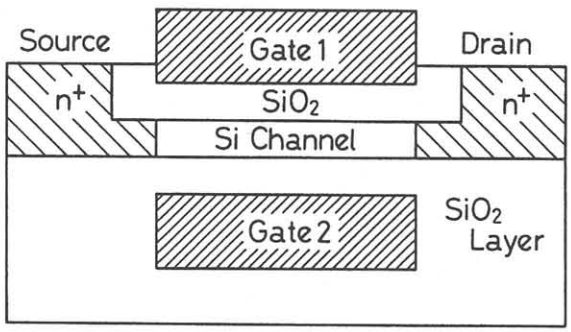

Fig.3. Dual gate SOI MOS junction.

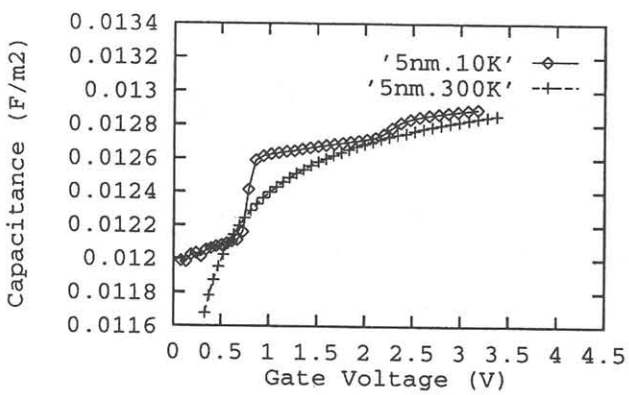

Fig.4. Computed C-V curve of the dual gate SOI MOS junction.

4. SUMMARY

The general features of nano-structure capacitance is analysed based on the self-consistent field approximation, and it is clarified that the capacitance is decomposed into three components serially connected. One is the extension of the capacitance of classical perfect conductors discussed in electrostatics. The quantum mechanical effect plays an important role in the other two components; one of them is proportional to the electronic density of states at the Fermi potential of the conductor in low temperatures. At the room temperature this portion is proportional to the electronic charge in the conductor. The other is due to the delocalization of electronic charge off the surface into the bulk of conductor. These two components have only the self-capacitance contributions. The diagrammatic expression of the capacitance network is developed for application to the electric circuit. The C-V curve of the dual gate SOI MOS junction was evaluated through computer simulation, and the presence and the characteristics of the nano-structure capacitance component are confirmed.

References

1) T.P.Smith et al., Phys. Rev., **B 32**, 2696 (1985).
2) M.Büttiker et al., Physics Letters, **A 180**, 364 (1993).