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ULSI Technology Evaluation and Precautions: A Novel View of SiO_2 Layer Properties in the nano- and Sub-Nanoscale.

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The Silicon dioxide/Silicon (OS) system is the center of interest for the development of Silicon devices and Si Integrated Circuits (IC). The progress of Technology and the scalling of devices need more and more thin oxide, or generally insulator layers (d_i<10 nm) /1,2/. Modern ULSI Technology demands elaboration of high precision and sophisticated methods for control and evaluation of OS-systems on nano- and sub-nanoscale, that was the main goal of our reserches.

We succeded to elaborate a new experimental approach to investigation and control of insulator layer/semiconductor(semimetal) system (IS) and to get at the first time "in-depth" nano- and sub-nanoscale distribution of the intrinsic charged traps throughout thin and ultra-thin SiO2 layer on Si. Detailed "in-depth" distribution of donor- and acceptor-type traps into SiO2 films on single crystal of Si have been measured by the Combined Field Effect in Electrolytes (CFEE) method /3-5/, the etch-back technique, and the ellipsometry. The CFEE-method enabled to registrate the volume density of electron/hole traps throughout thin and ultra-thin dielectric in the range $\rho = 10^{15} - 10^{21}$ el.cm^{-3} and some other parameters of the system of question with the thickness resolution about 0.1 nm.

The samples were prepared on (100) surface of p- and n-Si (4-11 Ohm.cm) wafers by two technologies after standard planing and cleaning procedures. The first group of OS-structures (Middle Temperature Oxide - MTO) was prepared by the ECR plasma-oxidation at the temperature of substrate 400°C; and the second group (High Temperature Oxide - HTO) - by the thermal oxidation in dry O_2, T = 1050°C. All samples were not annealed and the thickness of SiO2 layers was varied from 10 nm to 60 nm.

Total positive electric charge at the Si/SiO2 interface was Q_{tot} =+(5.61+ 0.41).10^{11} el.cm^{-2} for the MTO samples and Q_{tot} =+(4.55+ 0.26).10^{11} el.cm^{-2} for the HTO specimens. The samples of MTO group had the main maximum of fast electronic surface states density into the upper half of the band gap $E_{ss} - E_v$=0.7 eV. But the specimens of HTO series had the main maximum of surface states density into the down half of the band gap $E_{ss} - E_v$= 0.4 eV and more weak maximum into the upper half of band gap $E_{ss} - E_v$= 0.7 eV. Its surface density decreased sharply when the thickness of SiO2 becomes smaller than 1.0 nm for bouth oxides.

Independently of the initial oxide layer thickness the distribution of intrinsic charged traps had some common features for two types of oxide (Fig.1). There are three zones of the intrinsic traps location -"A", "B", and "C" through SiO2 layer. The first zone "A" of total thickness 5- 6 nm near Si/SiO2 interface includes three sub-zones of charged traps density distribution: donor-type traps with maximum density ρ = +(0.3 - 1.8).10^{18}el.cm^{-3} into an interval x_i = 4.0 - 6.0 nm from the Si/SiO2 interface; acceptor-type traps with maximum density ρ = -(0.5-3.0).10^{18}el.cm^{-3} at x_i = 2.0 - 4.0 nm; dramatic rise of the positively charged traps density to ρ =+(0.7 - 2.0).10^{19}el.cm^{-3} into the sub-zone with coordinates x_i = 0.2 - 2.0 nm.

Totally ignored in earlier experiments the zone "C" of charged intrinsic traps location is situated at the SiO2/Air interface into an interval 4 - 6 nm. It consists of two (or three) sub-zones: sub-zone of positively charged traps with ρ =+(1 - 3).10^{17}el.cm^{-3} is the nearest to the interface under discussion; sub-zone of negative traps with ρ =-(0.5 - 3.5).10^{17}el.cm^{-3}, and another possible sub-zone of donor-type traps with ρ =+(0.3 - 1.5).10^{17}el.cm^{-3} are more remote correspondently from the SiO2/Air interface (Fig.1).

There is verty low charged traps density $\rho < |\pm 3.10^{16}$el.cm$^{-3}|$ into the middle chemically and structurally uniform (Fig.2) part of SiO2 layers - zone "B" (Fig.1).

"In-depth" localization of intrinsic charged traps throughout zones "A", "B", "C", and its sub-zpnes descriptively correlates with "in-depth" distribution of the SiO2 layers etching velocities (v_{dis}) measured at the same time in our experiment (Fig.2) and partly supports of / 6,7 /.

The principle cause of "A"-zone creation is the misfit of Si and SiO2 crystallographic structures / 3 / and the compressive stress into the SiO2 zone the nearest to Si/SiO2 interface. This zone prescribes the quality and the perfectness of MOSFETs. The main causes of the "C"-zone generation are adsorption, diffusion, and chemical interaction of atmosphere components (H2O, CO2, O_2)

with the free outside surface of SiO2 layers as soon as its are formed. From our point of view the zone-"C" is responsible on the reliability of MOSFET IC.

The nano- and sub-nanoscale approach to important electric and physical-chemical properties of Si/SiO2 or in general SC(SM)/insulator structures realized by the CFEE-method allows to give more justified and comprehensive interpretation for many experimental results received earlier, taking in consideration physics, structure, end chemistry of such systems /3/.

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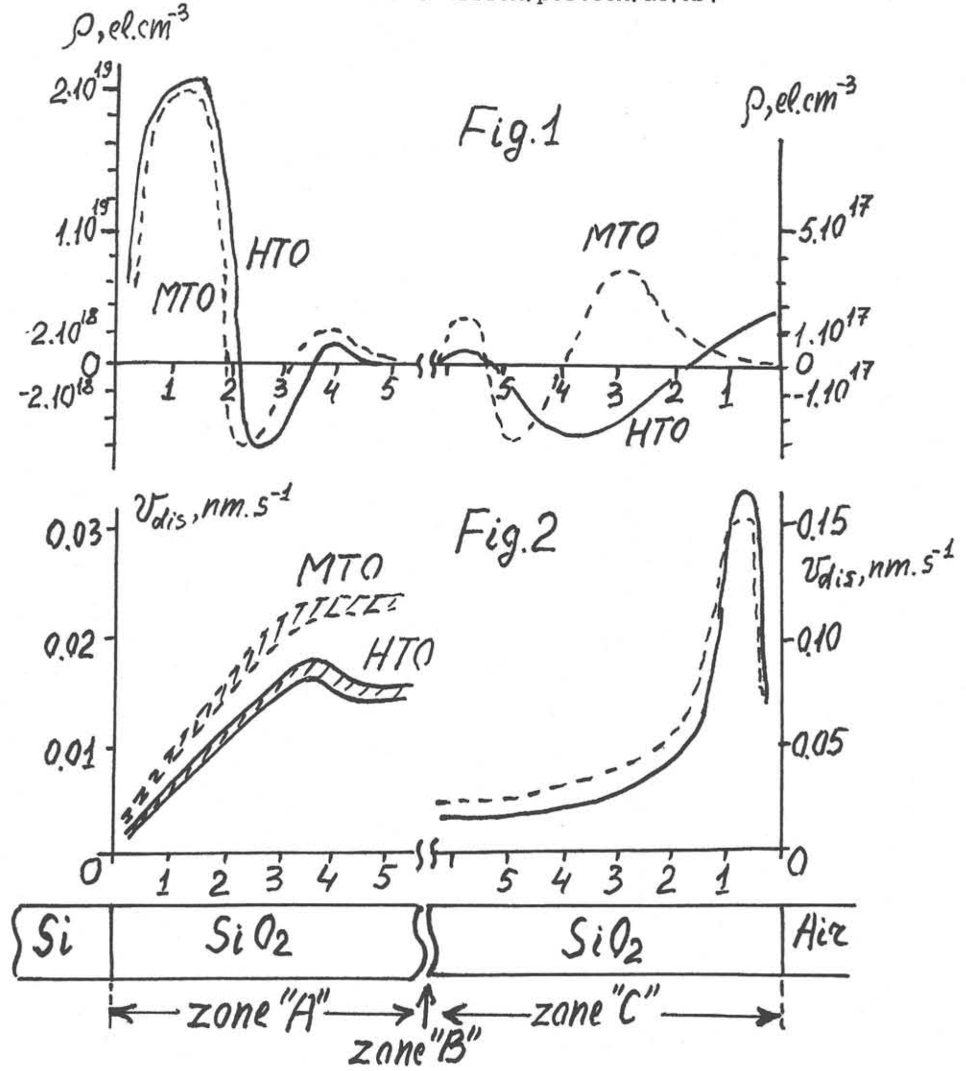

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