

Reduction of Threading Dislocation Density in InP-on-Si Heteroepitaxy with Strained Short-Periods Superlattices

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InP-on-Si heteroepitaxy is an important technique to realize the optoelectronic integrated circuits(OEICs) which consist of InGaAsP/InP optical devices and Si integrated circuits. Previously, room-temperature continuous-wave operation of an InGaAsP 1.5- μm -wavelength laser diode fabricated on the InP-on-Si heterostructure has been reported¹⁾. In their report, in order to reduce the threading dislocation density, very thick InP buffer layers ($>10\ \mu\text{m}$) were grown on the substrates and thermal cycle annealing was carried out. However, for OEIC application, thin buffer layers are required to integrate the optical devices on the Si substrate using conventional planar technology. Recently, in GaAs-on-Si and InGaAs-on-GaAs heteroepitaxies with multi-strained short-period superlattices (SSPSs), we found that the epilayers were grown two-dimensionally, and the generation of threading dislocations was suppressed by confining dislocations within hetero-interfaces^{2,3)}. Thus, we applied the $(\text{InAs})_m(\text{GaAs})_n$ SSPSs and the $(\text{GaAs})_j(\text{GaP})_k$ SSPSs to the InP-on-Si heteroepitaxy, in order to suppress the generation of threading dislocations.

Figure 1 illustrates the schematic drawing of the sample structure grown by molecular beam epitaxy. Firstly, a 400-nm-thick GaP layer was grown on Si(100) substrate misoriented by 4° toward [011] at a substrate temperature of 580°C . Then $(\text{GaAs})_j(\text{GaP})_k$ SSPSs and GaAs layer were grown on GaP/Si structure at 500°C . The numbers of monolayers (j,k) were changed in the order of (1,3), (1,1) and (3,1). After that, $(\text{InAs})_m(\text{GaAs})_n$ SSPSs were grown on the GaAs/SSPSs/GaP/Si heterostructure at 420°C . The numbers of monolayers (m,n) were changed in the order of (1,4), (1,3) and (1,2). The thicknesses of each SSPS and GaAs layer were 200 nm respectively. Finally, a 1- μm -thick InP layer was grown at 420°C . In order to evaluate the smoothness of the grown surfaces, reflection high-energy electron diffraction (RHEED) patterns were in-situ monitored during growth. The dislocations in the epilayer were observed by transmission electron microscopy (TEM).

Figure 2 shows the RHEED patterns during growth of InP/SSPSs/GaAs/SSPSs/GaP/Si heterostructure. Streaky patterns were maintained with no apparent transition to 3D spot patterns during the growth of the SSPSs, GaAs and InP layers. This means that each layer on the GaP/Si structure was grown two-dimensionally. Figure 3 shows the cross-sectional TEM images of the InP/SSPSs/GaAs/SSPSs/GaP/Si and the InP/GaP/Si heterostructures. Compared to the threading dislocations in the InP/GaP/Si structure, those in the InP/SSPSs/GaAs/SSPSs/GaP/Si structure were reduced remarkably by applying the multi-SSPSs to the InP-on-Si heteroepitaxy. Figure 4 shows the tilted TEM images of the InP/SSPSs/GaAs/GaP/Si structure. The hetero-interfaces can be observed by tilting the specimen. Misfit dislocations lying at hetero-interfaces were observed, as shown in Fig. 4. Most of these dislocations were propagated along $\langle 011 \rangle$ directions. On the other hand, no misfit dislocations running to $\langle 011 \rangle$ directions were observed at InP/GaP interface in the InP/GaP/Si structure. In conclusion, it was found that the generation of threading dislocations could be reduced by introducing a relatively thin buffer layer (1.8 μm) including multi-SSPSs at InP/Si hetero-interface, in spite of very large lattice mismatch (8%).

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2) T. Kawai, H. Yonezu, Y. Ogasawara, D. Saito, and K. Pak, Appl. Phys. Lett. **63**, 2067 (1993).

3) Y. Takagi, H. Yonezu, T. Kawai, K. Hayashida, K. Samonji, N. Ohshima, and K. Pak, J. Cryst. Growth **150**, 677 (1995).

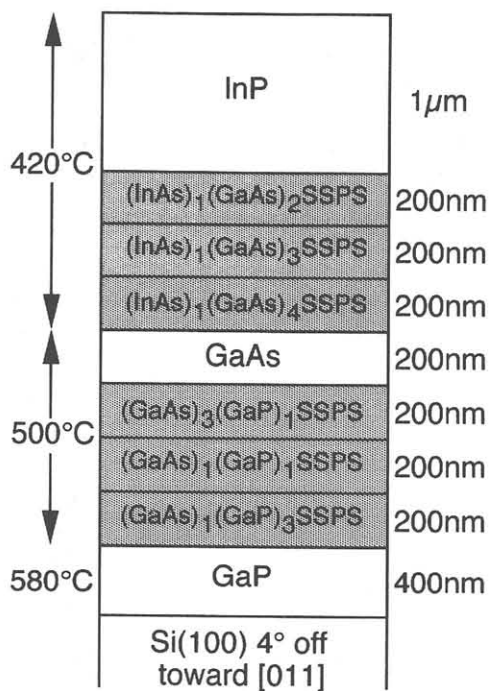


FIG. 1. Schematic drawing of the InP/SSPSs/GaAs/SSPSs/GaP/Si structure grown by molecular beam epitaxy.

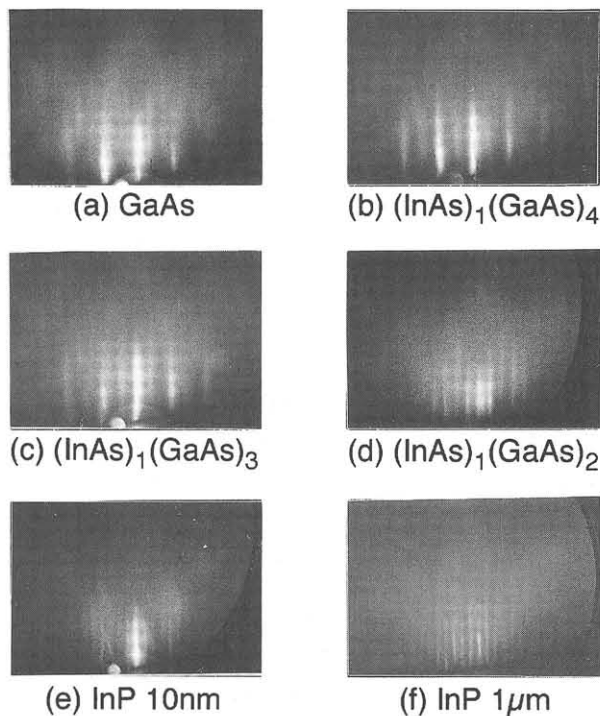


FIG. 2. RHEED patterns during growth of the InP/SSPSs/GaAs/SSPSs/GaP/Si heterostructure. These patterns were observed along $[011]$ azimuth.

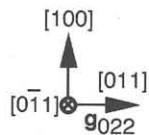
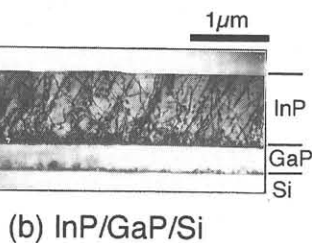
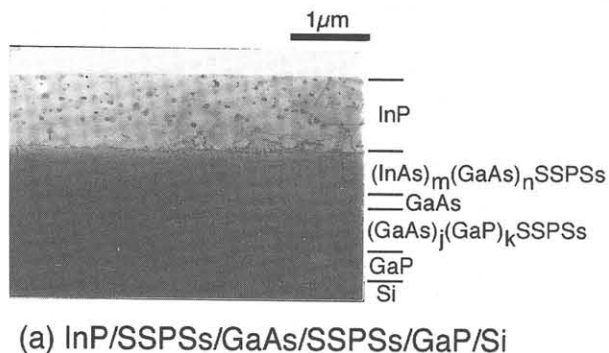


FIG. 3. $[0\bar{1}1]$ cross-sectional TEM images of (a) the InP/SSPSs/GaAs/SSPSs/GaP/Si structure and (b) the InP/GaP/Si structure.

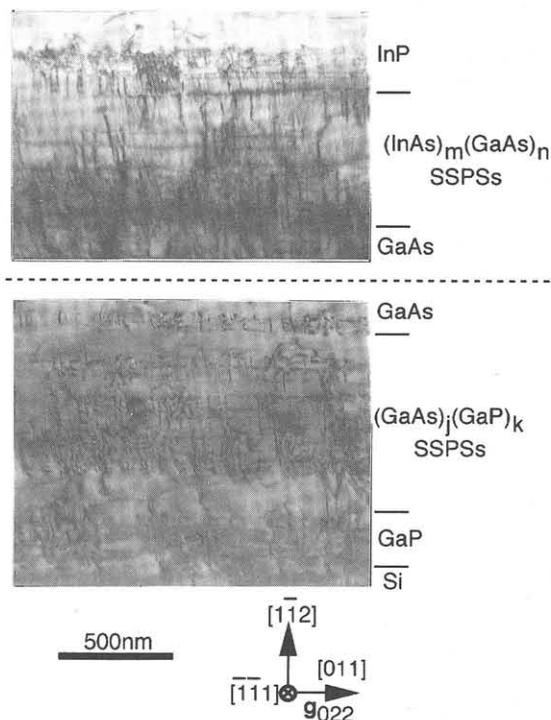


FIG. 4. Tilted TEM images of the InP/SSPSs/GaAs/SSPSs/GaP/Si structure. The sample was tilted at about 30° .