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Ferroelectric Nonvolatile Memory Technology and Its Applications

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Nonvolatile memory utilizing ferroelectric material is expected as a ultimate memory due to its low power operation and fast access in principle. Here we describe basic characteristics and reliability evaluation results of ferroelectric capacitor formed with spin-on and Liquid Source Misted Chemical Deposition (LSMCD) method, design of ferroelectric memory cell and applications for the ferroelectric nonvolatile memory.

1. Introduction

Ferroelectric material for nonvolatile memory has been researched and developed since the middle of 1980's mainly in the U.S.A.[1]. In 1990's triggered by the invention of a ferroelectric material of Bi based layered perovskite oxide [2] so called "Y1" that improved fatigue: degradation of polarization after a number of switching cycles, many companies and research institutes accelerated their activities toward the commercialization of the memory utilizing ferroelectric thin film.

We describe ferroelectric nonvolatile thin file technology first and its applications afterward.

2. Integration of Ferroelectric and CMOS

Ferroelectric thin film is formed after standard CMOS transistor and planalization processes as shown in figure 1. There exist some techniques for ferroelectric thin film deposition, exemplified by spin-on method, LSMCD, sputter and metal organic chemical deposition. Since we believe spin-on method is the closest technique to production use, we mainly show the data of this method. A source material for spin-on method can be adjusted to have arbitrary composition of metal organic components in a ferroelectric material. The source material is spun on and crystallized in oxygen gas. This method has a disadvantage of step coverage but has advantages of controllability of stoichiometry and short turn around time. This is suitable for low to middle density devices.

Ferroelectric process does not affect characteristics of CMOS transistors due to its maximum heat treatment of 800 ℃ so that there is no change in performance of microcontroller and other CMOS devices. This is an obvious advantage of ferroelectric process compared with an electrically erasable and programmable read only memory (EEPROM) or a dynamic random access memory (DRAM) that need dedicated CMOS process steps.

3. Basic characteristics of ferroelectric capacitor

Figure 2 and figure 3 shows the polarization and breakdown characteristics of ferroelectric capacitors respectively. According to the data, there is no dependence on capacitor area and enough charge can be obtained even for a 4M bit class memory cell.

4. Reliability of ferroelectric capacitor

One of the issues on reliability of ferroelectric capacitor is fatigue. The fatigue-free number of write cycles of ferroelectric capacitor is much greater than that of EEPROM that is typically 10^4 to 10^6. However in a ferroelectric memory the capacitor is switched not only by write operation but also by read operation, so called destructive read, and the fatigue is real issue for the memory of lead zirconate-titanate (PZT). Bi based layered perovskite oxide, for example $SrBi_2Ta_2O_9$, is not affected by the oxygen vacancy considered one of fatigue causes due to its layered perovskite oxide structure and shows good fatigue-free characteristics as

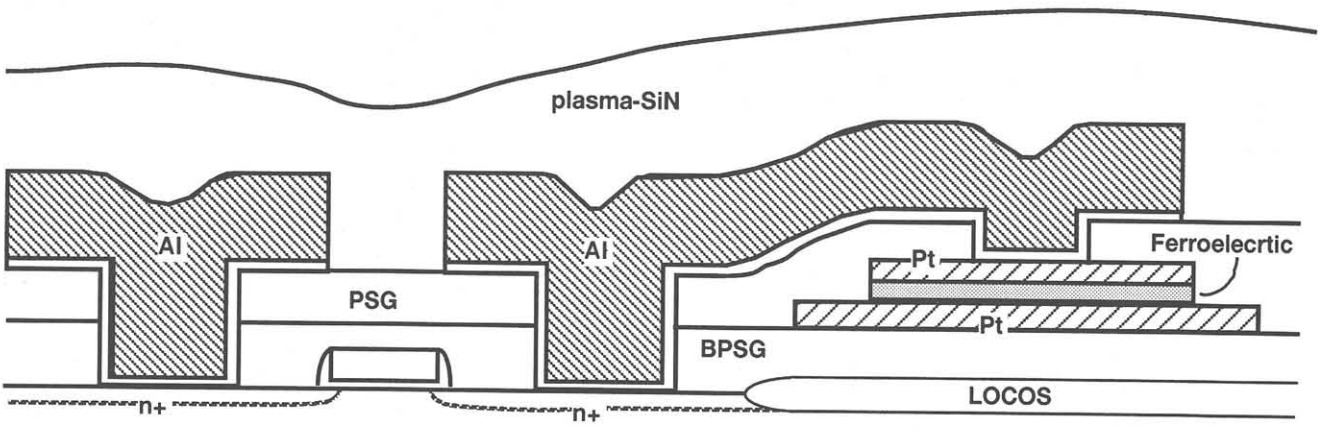

Fig. 1 Cross section of ferroelectric memory cell

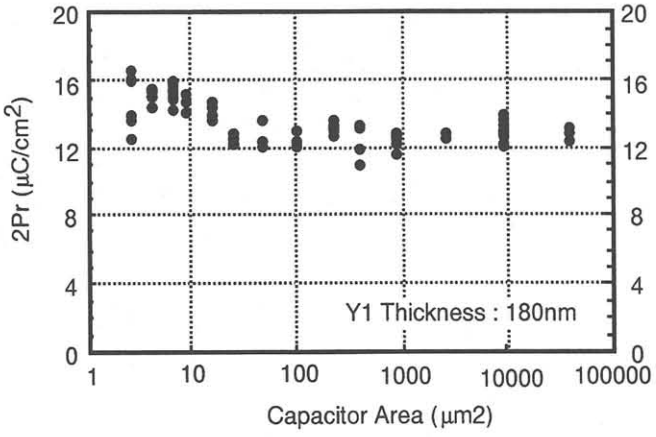

Fig. 2 Polarization of a ferroelectric capacitor

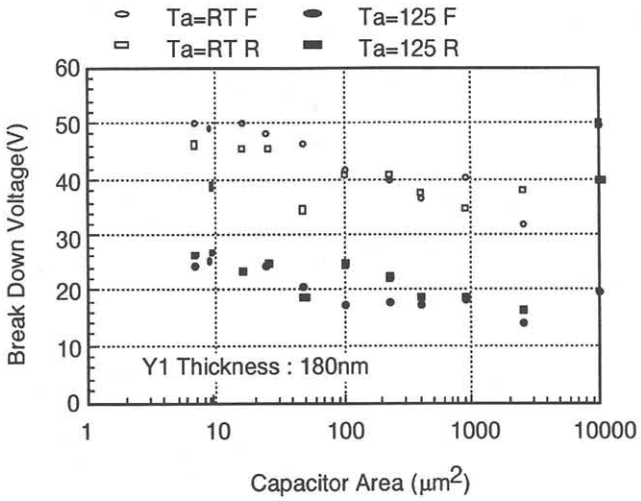

Fig. 3 Break down voltage of a ferroelectric capacitor

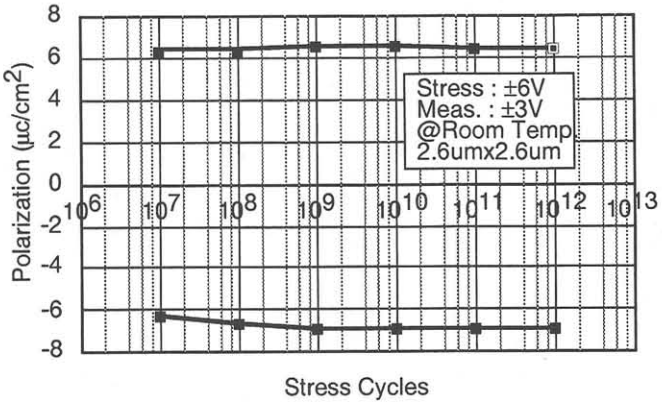

Fig. 4 Ensurance characteristice

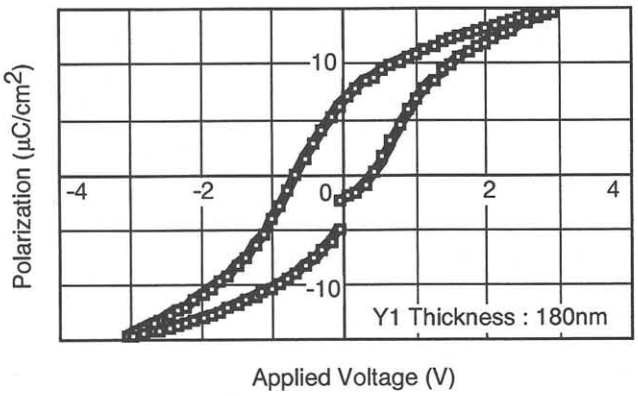

Fig. 5 Relaxation of hysteresis

shown in figure 4.

Ferroelectric material is known to have so called "imprint" characteristics. Imprint is the phenomena that after applying repetitious one directional pulses or DC voltage, hysteresis curve shifts along with the electric field axis. Hysteresis with imprint coincides well with initial one by applying some voltage offset. This implies that imprint is the results of fixed polarization and internal field caused by which remains even at 0V external voltage.

5. Memory cell design

Ferroelectric nonvolatile memories to date have mainly used 2T2C cell configuration consisting of 2 transistors and 2 capacitors for a bit. The cell operates stably because of its complimentary operation of a pair of 1 transistor and 1 capacitor.

On the other hand 1 transistor and 1 capacitor (1T1C) cell for a bit is strongly required for high density memory. The 1T1C cell needs a reference cell that generates a reference voltage for a sense amplifier to amplify small signal. Figure 5 shows preset reference cell we proposed [3].

Considering necessity of coincident characteristics of a reference cell with a memory cell in terms of temperature dependence, cell area deviation etc., it is desirable to use a ferroelectric capacitor for the reference cell. Ferroelectric thin film has so called "relaxation" effect: degradation of polarization after a certain period as shown in figure 5. It is required to take account of this relaxation into the design of the memory cell and reference cell as well as their dependence on applied voltage and temperature etc.

The ratio of bitline parasitic capacitance to equivalent cell capacitance determines sensing voltage on a bitline. We have to pay attention to the ratio especially in the case of a low density memory in which the bitline capacitance is relatively small hence the small ratio causing small sensing voltage. In this sense research on an accurate circuit model of ferroelectric capacitor is very important.

6. Advanced technology

One of the candidates of ferroelectric thin film deposition for high density devices is LSMCD. In the LSMCD single spin-on liquid source is misted, carried to a chamber with carrier gas and deposited on a substrate. Drying process and crystallizing process in oxygen gas conform to those of spin-on method. The LSMCD has better step coverage essential for higher integration and the same controllability of stoichiometry as the spin-on method because of single liquid source.

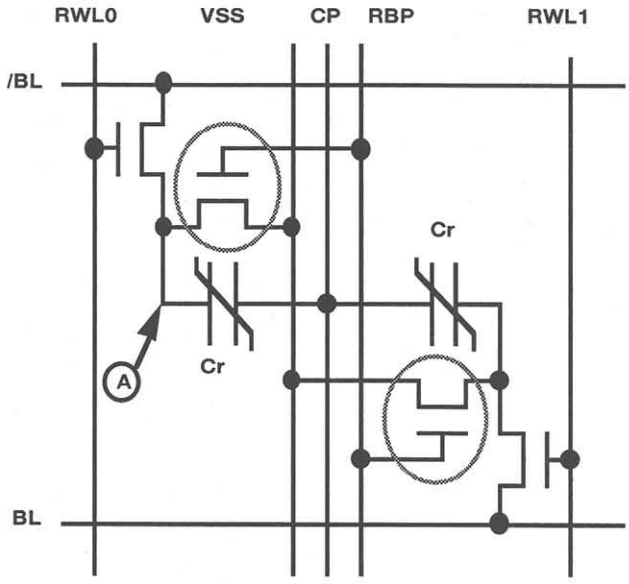

Fig.6 Preset reference cell

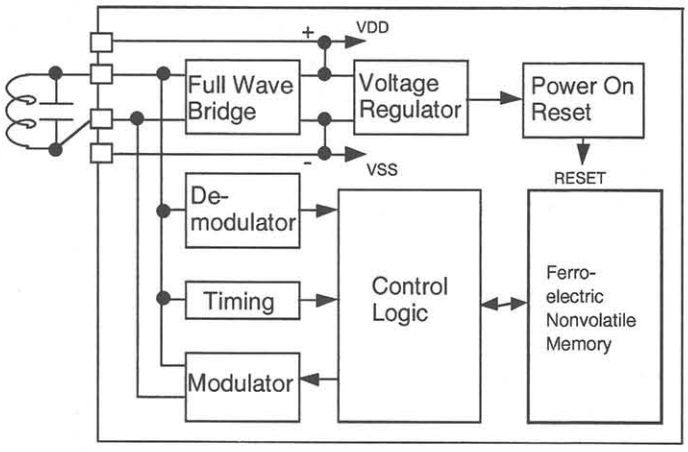

Fig. 7 RF-ID tag chip

7. Applications of ferroelectric memory

Ferroelectric nonvolatile memory is researched and developed not only for a stand alone memory but also for an embedded memory because of its lower power requirement, faster access time and potentially lower cost. A radio frequency identification (RF-ID) tag chip is one of this sort of applications. The chip generates DC power voltage by rectifying carrier electromagnetic field and accesses on-chip ferroelectric nonvolatile memory to read and write. The communication rage is longer than that with EEPROM since the tag chip based on ferroelectric memory consumes less power and operates at lower supply voltage in week electromagnetic field (figure 7).

Other application for a microcontroller is shown in figure 8. The microcontrollers constructed to date have EEPROM as a reprogramable memory and a full CMOS static random access memory (SRAM) for data processing on the chip. SRAM has large cell area and EEPROM cannot be used as a data memory due to slow write speed. If you want another chip with different SRAM to EEPROM memory capacity ratio, the chip has to be redesigned. A ferroelectric memory embedded microcontroller[4] has much flexibility because it can use the ferroelectric memory as a main memory. The memory area is used for boost program and as data and work area, but there is no physical segmentation among those areas. It is not necessary to design many variety of microcontroller chips. Furthermore it is possible for the microcontroller to have evolving program by having nesting function inside the program itself which generates new program data.

8. Summary

We described ferroelectric thin file deposition technology, its characterization, ferroelectric memory cell design and applications of ferroelectric memory. Ferroelectric technology has not yet caught up the most advanced semiconductor technology, however we believe that it will have very important role in the field of semiconductor devices due to its superior characteristics.

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References

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4) T. Sumi, et al.: ISSCC Digest of Technical Papers (1995) 70

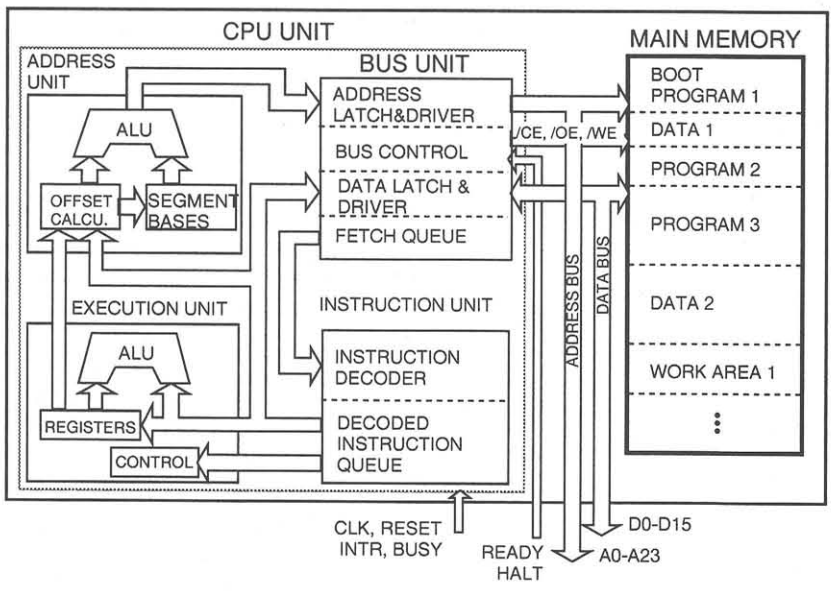

Fig. 8 Ferroelectric nonvolatile memory embedded microcontroller