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Low-Thermal-Budget Process-Controlled Monolayer Level Incorporation of Nitrogen into Ultra-Thin Gate Dielectric Structures: Applications to MOS Devices

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A low-temperature/low-thermal-budget process for incorporation of nitrogen (N-) atoms into ultra-thin SiO_2 dielectrics is presented. This approach combines plasma-assisted oxidation/nitridation and film deposition steps, with rapid thermal annealing, providing independent control over concentrations and spatial distributions of the N-atoms, and structural and chemical relaxation processes that minimize defects and defect precursors. As an example, we demonstrate that monolayer N-atom incorporation at Si-SiO_2 interfaces increases reliability with respect to interfaces formed by thermal oxidation.

1. INTRODUCTION

There is considerable interest in incorporating N-atoms into ultra-thin (3 to 5 nm) gate dielectrics. In devices incorporating ultra-thin dielectrics, defect generation processes that limit device reliability occur in the immediate vicinity of the Si-SiO_2 interface,[1] so that N-atom incorporation at this interface has drawn much attention. To optimize overall device performance and reliability, it may also be necessary to control the spatial distribution of N-atoms in other portions of the dielectric structures. For example, the presence of N-atoms can effect device performance in ways that are directly correlated with their concentration profiles;

i) at the Si-SiO_2 interface - by minimizing the densities of interface traps (D_{it}) and fixed charge (Q_{ss}) defects, and by improving reliability;

ii) within the bulk of the dielectric films - by increasing the effective dielectric constant, thereby allowing the use of thicker films with reduced oxide equivalent thicknesses; and

iii) at the poly-Si-SiO_2 interface - by blocking boron (B-) atom diffusion from p^+-doped poly-Si gate electrodes into and through the dielectric to the Si-SiO_2 interface.

These effects of N-additions have in part been verified in devices fabricated by high-temperature oxidation, nitridation and re-oxidation methods at processing temperatures in excess of 1000°C, and in some instances up to 1200°C.[2-7] However, these high temperature processes cannot control separately the amount of bonded-N and its spatial distribution with respect to the Si-SiO_2 interface, while at the same time controlling the overall dielectric film thickness in the required 3-5 nm thickness regime. This is because high-temperature approaches require three microscopic processes to take place simultaneously: i) cracking of N-containing source gases, ii) incorporation of N-atoms into the dielectric and/or at the Si-SiO_2 interface, and iii) growth of an ultra-thin film. The research reported here accomplishes N-atom incorporation by a low-temperature. low-thermal-budget approach using i) low-temperature (300°C) plasma-assisted processing to control N-atom distributions within dielectric films and/or at Si-SiO_2 and SiO_2-poly-Si interfaces, and ii) low-thermal-budget rapid thermal annealing (RTA), e.g., at 900°C for 30 s, to promote chemical and structural relaxations required to minimize densities of defects, and defect precursors. In previous studies,[8] RTA induced chemical relaxations were used to eliminate bonded-H that derived from use of H-containing source gases such as SiH_4 and NH_3; whilst structural relaxations promoted recombination of Si and N-atom dangling bonds produced by H-atom evolution.[9]

2. PROCESSING APPROACH

In this paper, we present an important modification of this approach to device processing in which, non-H containing N-atom source gases, such as N_2 and N_2O, are used in place of NH_3. This has resulted in significant decreases in bonded-H in bulk oxynitride and nitride films, at the Si-SiO_2 interface, and in addition have helped develop new approaches for incorporation of N-atoms at Si-SiO_2 and SiO_2-poly-Si interfaces. We have obtained N-atom concentrations:[10]

i) between ~1.5 and 9×10^{14} cm^{-2} at Si-SiO_2 interfaces by plasma-assisted oxidation in N_2O with defect densities and breakdown fields comparable to furnace oxides, and with improved reliability with respect to interfaces formed by thermal oxidation;

ii) at alloy, and compound levels in oxide-nitride-oxide and oxide-oxynitride-oxide dielectrics with oxide equivalent thicknesses to ~4 nm, while maintaining electrical performance and reliability equivalent to devices with thermally-grown oxides;[11,12] and

iii) of the order of 5-50 at.% at the top of the uppermost oxide layer of multilayer dielectrics by plasma-assisted nitridation that yields ~2 to 3 nitrided layers.[11,13]

3. N-ATOMS AT Si-SiO_2 INTERFACES

We discuss two device structures: i) metal-oxide-semiconductor (MOS) capacitors with Al-gate electrodes, and

ii) field effect transistors (FETs) with phosphorus doped poly-Si gate electrodes. For the MOS capacitors, the substrates were p/p^+ Si (100) wafers with an epi-layer resistivity of ~10 Ω-cm; lower resistivity wafers with hole concentrations, p~$4x10^{17}$ cm^{-3} were used for the FETs. In situ processing began with a 300°C plasma-assisted oxidation step in either O_2, N_2O or N_2O/O_2 mixtures. For MOS capacitors, the pre-oxidation treatment was a *standard*, high temperature, RCA clean terminated by an HF-rinse; for the FETs, the Si surface was not subjected to an RCA clean; instead, a field oxide about 200 nm thick was grown, and the gate oxide regions were opened up by a combination of low-pH and dilute HF etches. For MOS capacitors, 15 nm of SiO_2 was then deposited by remote PECVD at a pressure of 300 mTorr and a temperature of 300°C by excitation of He (200 sccm) and N_2O (20 sccm) in an upstream rf plasma upstream; 2 sccm of 10% SiH_4 in He was introduced downstream. For FETs, both N_2O and O_2 were used in the deposition of 5.5 nm of SiO_2 by similar 300°C remote PECVD processes. MOS capacitors were fabricated using Al-gate electrodes; patterning was by standard photolithographic techniques, maximum processing temperatures of 400°C). FET structures used phosphorus-doped poly-Si gate electrodes processed at 900°C.

AES and SIMS were performed on wafers dedicated to interface characterization. AES measurements were performed on-line in a surface analysis chamber immediately after the plasma oxidations; the SIMS depth profiles were made after the oxide depositions. The AES Si_{LVV} peak at 92 eV is due to Si-Si bonds and is identical for samples. After an RCA clean/HF rinse, H-terminated Si surfaces displayed C and O contamination. After a 2 min exposure to a remote H_2 plasma, C contamination was reduced below the AES detection limit, and the O was also reduced. C was reduced below AES detection by a 15 s exposure to an O_2 plasma, or by a 30 s exposure to an N_2O plasma with a concurrent plasma-assisted growth of ~0.5-0.6 nm of SiO_2.[10,14] Exposure to the N_2O plasma also produced a detectable N AES signal that was consistent with N-Si bonds being within two-three molecular layers of the Si-SiO_2 interface.

Areal densities of the N, C and F at the Si-SiO_2 interfaces were determined by integration of the respective mass signals in the SIMS data,[14] which showed that each of three plasma treatments reduced residual C-contamination to about the same level of $(2\pm0.5)x10^{12}$ cm^{-2}; F-atom concentrations were also in the 10^{12} cm^{-2} range The 15 and 30 s exposures to the N_2O plasma gave N concentrations, [N], of $(9\pm0.5)x10^{14}$ cm^{-2}, whilst 5 s and 15 s exposures to the O_2 plasma yielded [N] ≈ $(2\pm0.5)x10^{14}$ cm^{-2}. The sample exposed to the H_2 plasma had [N] ≈ $6x10^{14}$ cm^{-2}. Interfacial N after H_2 and O_2 treatments was derived from the N_2O source gas used in SiO_2 depositions. Combining SIMS and AES with studies of optical second harmonic generation,[15] we have concluded that N atoms identified above are *at* the Si-SiO_2 interface. SIMS and AES measurements were also performed on samples in which the oxidation step was done with N_2O/O_2 mixtures. C and F levels were comparable to those described above, and levels of N at the Si-SiO_2 interface scaled with the fraction of N_2O in the N_2O/O_2 mixture.

Table 1 includes results of conventional C-V and I-V measurements performed on MOS capacitors and FETs, respectively. Mid-gap D_{it} values did not correlate simply with the N concentration at the Si-SiO_2 interfaces. Interfaces formed by 2 minute exposures to the remote H_2 plasma resulted in a mid-gap D_{it} ~$2x10^{11}$ eV^{-1} cm^{-2}. A 5 s exposure to a remote O_2 plasma give mid-gap D_{it}'s of ~$7x10^{10}$ eV^{-1} cm^{-2}; this decreased to ~$1x10^{10}$ eV^{-1} cm^{-2} after a 15 s exposure. A similar trend was found for the remote N_2O plasma: a mid-gap D_{it} of ~$5x10^{10}$ eV^{-1} cm^{-2} for a 15 s exposure decreasing to ~$1x10^{10}$ eV^{-1} cm^{-2} after a 30 s exposure. We thus conclude that: i) comparable levels of D_{it} can be obtained by pre-deposition oxidation in either O_2 or N_2O, and ii) these low D_{it} values are obtained when the oxidation step is performed at sufficiently long times: 15 s for the O_2, and 30 s for the N_2O treatments. Comparisons with MOS capacitors with oxide layers formed by conventional thermal oxidation in dry O_2 at 900°C have demonstrated that D_{it} levels in optimized MOS capacitors with plasma-oxides and N-atom or O-atom terminated interfaces are comparable to those of the thermal oxides.

Table 1 Electrical Measurements of MOS and FET devices

(a) MOS Capacitors

Interface Treatment	D_{it} ($x10^{10}$ eV^{-1} cm^{-2})
O-atom terminated	1.0±0.5
N-atom terminated	1.0±0.5
NH-terminated (400°C)	20±5
NH-terminated (900°C)	1.0±0.5
thermally-grown oxide	1.0±0.5

(b) FETs

Interface Treatment with Plasma-oxide	Effective Mobility (cm^2/V-s)	Threshold Voltage (V)
O-atom terminated	375±10	0.39±0.03
N-atom terminated	375±10	0.39±0.03
thermally-grown oxide	375±10	0.39±0.03

Based on results for the H_2 plasma treatment, where oxidation proceeds in parallel with the initial stages of film deposition, we conclude that the oxidation treatment must be sufficiently complete to prevent oxidation during deposition that leads to significantly higher values of D_{it}. The results given above, combined with studies on devices with nitride and oxynitride composite dielectrics deposited from NH_3 indicate that N-atoms, as introduced above, and NH-groups, as introduced using NH_3 source gases,[8,9] behave very differently at Si-SiO_2 interfaces; i) N-atom terminations can promote defect densities as low as thermal oxides, whilst ii) NH-groups promote significantly higher levels of D_{it}, that can only be reduced after high temperature RTAs (typically 30 at 900°C)

in which the H-atoms are eliminated.[9)]

The beneficial effects of N-atom incorporation with respect to reliability at Si-SiO_2 interfaces are evident from stress bias studies on FETs. Before discussing these, it is important to understand effects of N-atom incorporation on transistor current-drive characteristics. This is illustrated in Fig. 1: i) where we show FET characteristics of devices with plasma-oxides, and both nitrided and non-nitrided interfaces, and ii) where these are compared with properties of devices with thermally-grown oxides (dry oxidation at 900°C). The highest drive currents were obtained in devices with the thermally-grown oxides, while devices with deposited oxides and nitrided interfaces displayed higher drive currents than devices without interface nitridation. The differences between the plasma-processed device with the nitrided-interface and the device with the thermal oxide are due in part to: i) dopant redistribution effects, as well as ii) inherent differences in interface strain, and strain induced relaxation.

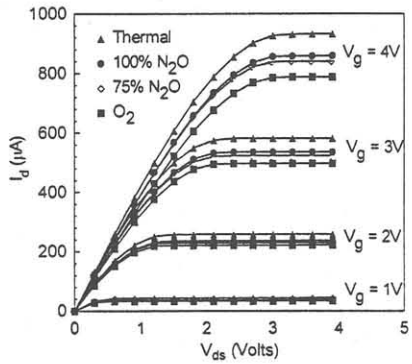

Fig. 1 Transistor current-voltage characteristics.

Figures 2(a) and 2(b) illustrate improved reliability that scales with increasing interface nitridation. We have studied $\Delta g_m/g_{m,max}$ and $\Delta V_t/V_t$, versus [N] where g_m is the transconductance, and V_t is the threshold voltage. In both instances, reliability for FETs with O-terminated interfaces with plasma oxides is poorer than for FETs with thermal oxides; however, reliability for devices with plasma oxides and N-terminated interfaces is improved with respect to FETs with thermal oxides.

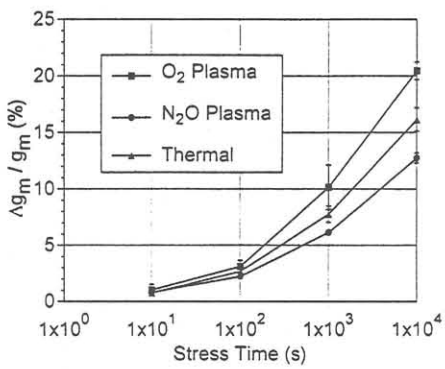

Fig. 2(a) $\Delta g_m/g_{m,max}$ as a function of stress time

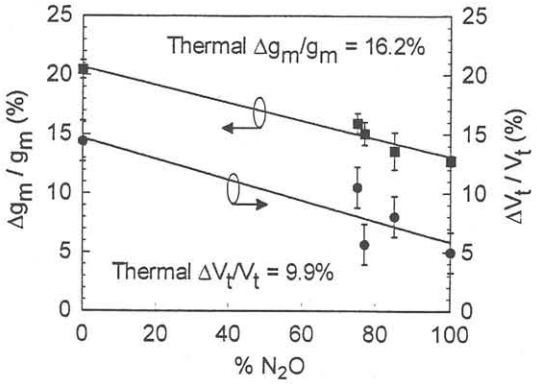

Figure 2(b) $\Delta g_m/g_{m,max}$ and $\Delta V_t/V_t$ as functions of the amount of nitrogen at the Si-SiO_2 interface.

4. SUMMARY

We have demonstrated specific benefits of monolayer N-atom incorporation at Si-SiO2 interfaces. From a comparison between the results in Fig. 1 with those in Figs. 2(a) and (b), we find that initial device performance and post-stress reliability are effected differently by N-atom additions.

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