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Interface States in Top Gate Metal-Silicon Nitride-Silicon Structures

J. Kanicki
Center for Display Technology and Manufacturing
The University of Michigan
2360 Bonisteel Blvd.
Ann Arbor, MI 48109, USA

S. Backert and N. Picard
Department of Solid State Physics
Ecole Polytechnique
91128 Palaiseau Cedex, France

Although it is known that the hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT) performance can be affected by the quality of the hydrogenated amorphous silicon nitride / a-Si:H interface, it is not experimentally simple to separate the contribution of the interface states from the a-Si:H bulk states. We have develop a experimentally simple capacitance method to separate capacitance due to the interface states from the observed total capacitance, which includes insulator capacitance and depletion layer capacitance; these interface states have been investigated using a metal / nitride / a-Si:H / c-Si (MNSS) structure. Using this capacitance method we were able to determine the distribution of localized density of interface states as a function of the energy for the N-rich nitride / a-Si:H structures having different a-Si:H film thicknesses. We have found that the tail states, which start with a high density close to the mobility edges, fall off vertically into the bandgap, and the states below the conduction bandtail states decease further exponentially to a minimum value, of about 1.2×10^{11} eV^{-1} cm^{-2} close to the Fermi level located at 0.75 eV below the conduction mobility edge. Then the interface density of states increase again with decreasing energy until we finally reach the valence band tail states. The width of the valence band tails is larger than the width of conduction band tails, and there is only one well defined peak in the distribution of the interface state density. This peak is located at about 0.96 eV above the valence band mobility edge, and is associated with the silicon dangling bonds present at nitride / a-Si:H interface. The important consequence of this result is that, on one hand, a low density of interface states in the top half of the gap leads to a steep prethreshold slope for positive bias, and, on the other hand, a high density of interface states in the bottom half leads to a low off-current for negative gate voltage in a-Si:H TFT using N-rich nitride as a gate dielectric.

Similar measurements reveal that the density of interface states in metal / nitride / c-Si (MNS) structures is much larger near the valence band than the conduction band edges, but no well defined peak density of interface states exists inside the c-Si energy gap. The influence of the substrate temperature, r.f. power density, and helium or hydrogen dilution on the interface density have been investigated. We have found that the density of the interface states, on one hand, decreases with increasing substrate temperature for a given r.f. power density, and, on the other hand, increases with increasing r.f. power density for a given substrate temperature. The He dilution does not improve the interface density but decreases the density of the fixed charges inside the silicon nitride film. The fixed charges are increasing function of both substrate temperature and r.f. power density.

We have also used this method to investigate the electrical instabilities induced by the bias-temperature-stress (BTS) in both MNSS and MNS structures. We have found that both creation of the interface states and the charge trapping in the nitride are responsible for the observed flat-band voltage shift in these structures. However, depending on the nature of BTS, one of the two mechanisms is more important than the other. Details of this very important and interesting BTS study will be given during the talk.

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Jerzy Kanicki : tel. 313-936-0964, fax: 313-936-0347.