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Oxynitride Pad LOCOS (ON-LOCOS) Isolation Technology for Gigabit DRAMs

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An advanced LOCOS-based isolation technology using oxynitride pad (ON-LOCOS) has been depeloped for gigabit DRAM. By using this simple isolation process, bird's-beak encroachment (BBE) and field oxide thinning is reduced. Defect-induced leakage and degradation of thin gate oxide were not seen. The devices with ON-LOCOS show excellent isolation characteristics and narrow channel effect is highly suppressed.

[Introduction]

Reducing device size toward the 1 to 4G DRAM generation is expected to require an isolation pitch of around 300nm[1]. Though there have been many reports on LOCOS-based isolation techniques for 256M - 1G generations[2-4], They tend to be much more complicated than conventional LOCOS and are not suitable for generations beyond the gigabit, because the most prominent benefit of using LOCOS-based isolation rather than high performance shallow trench isolation is process simplicity. Considering the gigabit generation, process simplicity should have priority over other characteristics.

In this paper, we present ON-LOCOS from this standpoint. ON-LOCOS imposes only slight nitridation before conventional oxide pad growth. By optimizing the nitridation process, bird's-beak enchroachment (BBE) of less than 50 nm with LOCOS thickness of 250 nm was achieved without stress-induced defects, making the technique applicable to gigabit DRAMs.

[ON-LOCOS Process]

The ON-LOCOS process starts with direct nitridation of silicon at 500-900℃ in NH_3/Ar for 10 minutes followed by oxidation in dry O_2 at 900℃ for 30 minutes, which results in formation of 3 nm-thick oxynitride. Fig. 1 shows nitrogen content in the oxynitride layer as a function of the nitridation temperature. The nitrogen content is controllable by changing nitridation temperature. After forming the oxynitride, 115 nm-thick nitride is deposited on it and patterned. Then the oxynitride layer at the silicon surface is removed using HF. Finally, 250 nm-thick field oxide is grown in wet O_2 at 1000℃. The ON-LOCOS process was integrated with a 0.18 μm gate-length high performance CMOS process[5], with a retrograde well (400 keV with $2x10^{13}/cm^2$ for phosphorus and 200 keV with $2x10^{13}/cm^2$ for boron), a 4 nm-thick gate oxide, and with an n^+ and p^+ dual-polysilicon gate process, comparable to the 1G generation.

[Results and Discussions]

A small BBE in a narrow active region is a major requirement in high-density DRAMs. Fig. 2 shows SEM top-views of ON-LOCOS (nitrogen content 17%) and

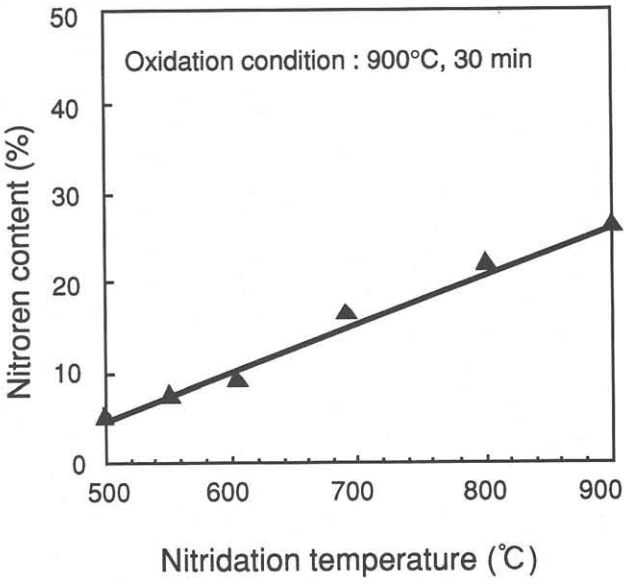

Fig. 1 Nitrogen content in the oxynitride layer as a function of the nitridation temperature.

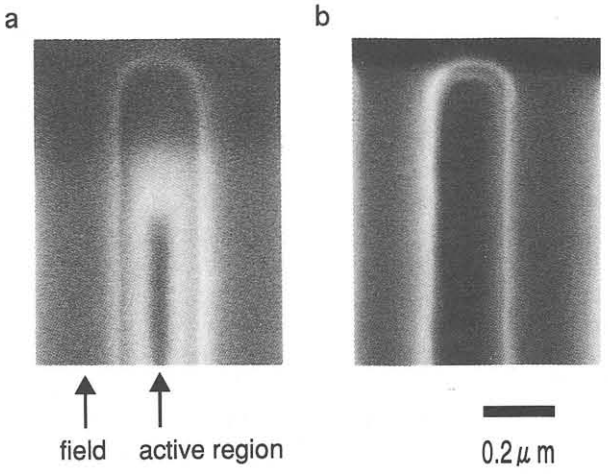

Fig. 2 SEM top-views of conventional LOCOS(a), and ON-LOCOS(b).

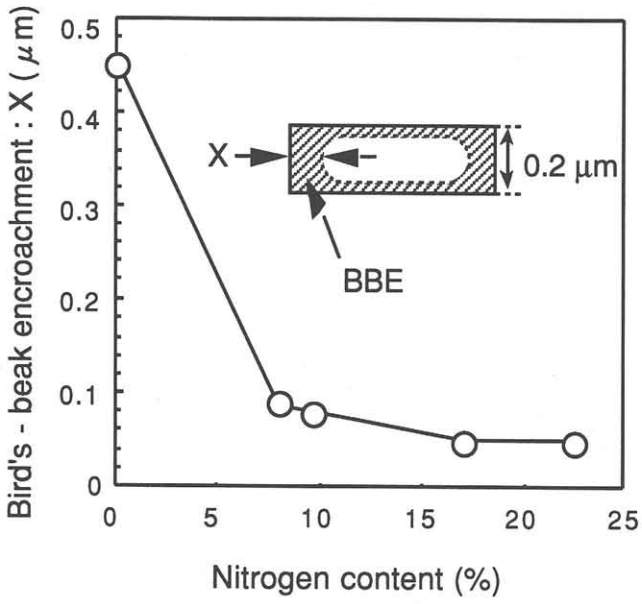

Fig. 3 BBE vs. nitrogen content in the oxynitride layer. Field oxide thickness is 250 nm.

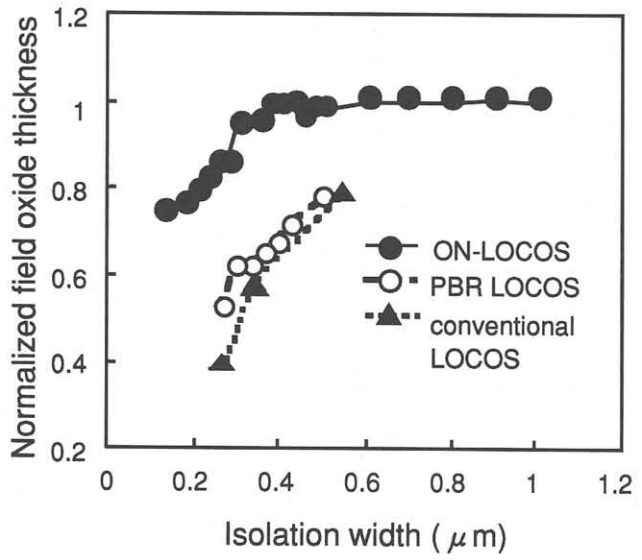

Fig. 4 Normalized field oxide thinning with ON-LOCOS, PBR LOCOS, conventional LOCOS.

conventional LOCOS. In the ON-LOCOS, the BBE is supressed independently of the mask pattern. Fig. 3 shows BBE vs. nitrogen content in the oxynitride layer for field oxide thickness of 250 nm. ON-LOCOS exhibits smaller BBE within 50 nm even around narrow pattern (0.2 μm), sufficient for 1-4G DRAMs. The oxynitride pad effectively prevents oxidant diffusion, resulting in suppression of the bird's-beak formation without sealing the pad edges with a complicated spacer formation(4).

The small pitch required by DRAMs must be accompanied by reduced field oxide thinning in order to achieve strict isolation characteristics and global planarity. Fig. 4 shows the plot of normalized field oxide thinning with ON-LOCOS, conventional LOCOS, and LOCOS-based isolation (PBR LOCOS) as previously reported(6)(7). ON-LOCOS reduces only 10%, compared to 50% for conventional LOCOS and 40% for PBR LOCOS for a drawn spacing of 300 nm. One possible reason for reduced oxide thinning is that oxidant species are effectively consumed to contribute to field oxide growth rather than bird's-beak growth.

The characteristics of less BBE and less field oxide thinning must not spoil junction characteristics or gate-oxide integrity. Junction characteristics are investigated using diodes with an area of 1.0×10^{-3} cm^2 and a perimeter of 0.13 cm. Fig. 5 shows n^+/p and p^+/n reverse junction characteristics. No difference is seen between the isolation techniques, indicating that no defects are induced by the ON-LOCOS process and that refresh characteristics will not degrade. Fig. 6 shows time-dependent dielectric breakdown (TDDB) characteristics. Q_{BD} of 63% cumulative failure is 10 C/cm^2. TDDB for ON-LOCOS is not inferior to that for conventional LOCOS. There is no defect generation resulting in the degradation of gate oxide.

Fig. 7 shows Al-gate field threshold voltage (V_{TF}) vs. n^+-n^+ and p^+-p^+ spacing with channel stop implantation conditions indicated. Both retrograde well and channel stop implants are performed after LOCOS process. Isolation to 0.25 μm can be achieved for the DRAM periphery.

The narrow-channel effect of 0.18 μm gate-length MOSFET was evaluated with various gate widths as shown in Fig. 8. The narrow-channel effect is highly suppressed by the channel stop doping profile formed after LOCOS formation and Vth of both type FETs remains unchanged until W=0.2 μm. In NMOS FETs, inverse narrow-channel effect is seen below 0.2 μm. This effect seems to be induced by the redistribution of the p-well profile due to the segregation phnomenon(8).

[Conclusion]

An oxynitride pad was used for conventional LOCOS for process simplicity and higher integration. Bird's-beak encroachment was within 50 nm and field oxide thinning was 10% for a drawn spacing of 300 nm, which is applicable to gigabit-generation DRAMs. Defect-induced leakage and degradation of thin gate oxide were not seen. Isolation characteristics and reduced narrow-channel effect reveal that this simple ON-LOCOS technique has high potential for gigabit-generation DRAMs with low process cost.

[References]

(1) A. Bryant, et al., IEDM Tech. Dig., p. 671, 1994.
(2) D. H. Ahn, et al., IEDM Tech. Dig., p. 679, 1994.
(3) T. Kaga, et al., IEDM Tech. Dig., p. 927, 1994.
(4) J. Pfiester, et al., VLSI Symp. Dig., p. 139, 1993.
(5) T. Yamazaki, et al., IEDM Tech. Dig., p. 906, 1993.
(6) T. Park, et al., SSDM. Dig., p. 528, 1993.
(7) N. Shimizu, et al., IEDM Tech. Dig., p. 279, 1992.
(8) K. Ohe, et al., IEEE Electron Device Lett., p. 636, 1992.

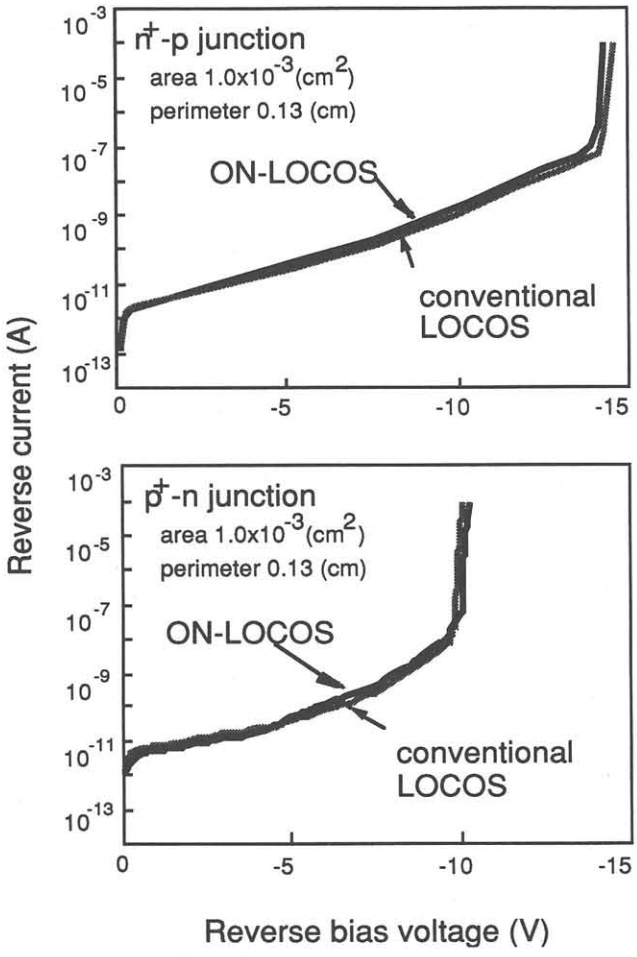

Fig. 5 n^+- p and p^+- n reverse junction characteristics of ON-LOCOS and conventional LOCOS.

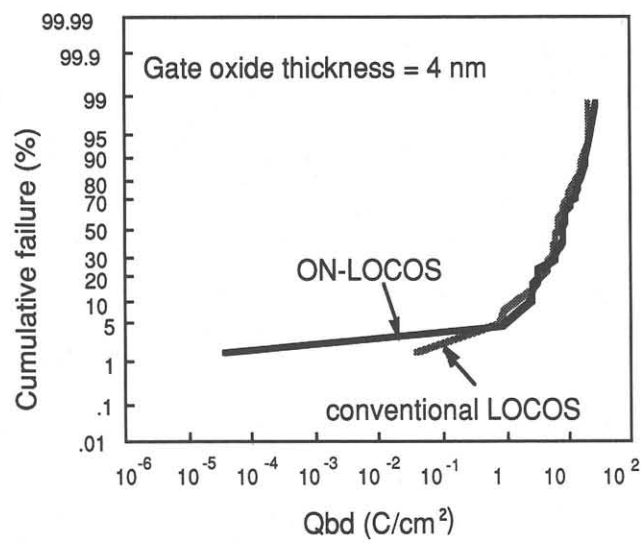

Fig. 6 Time-dependent dielectric breakdown(TDDB) characteristics of ON-LOCOS and conventional LOCOS.

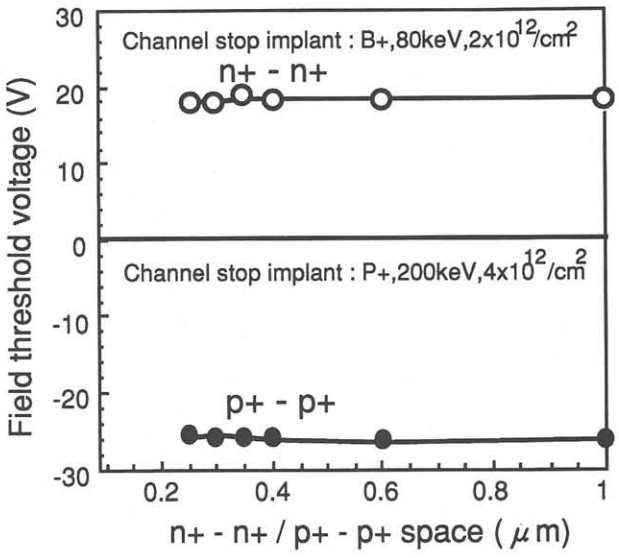

Fig. 7 Al-gate field threshold voltage (V_{TF}) vs. n^+- n^+ and p^+- p^+ space with ON-LOCOS.

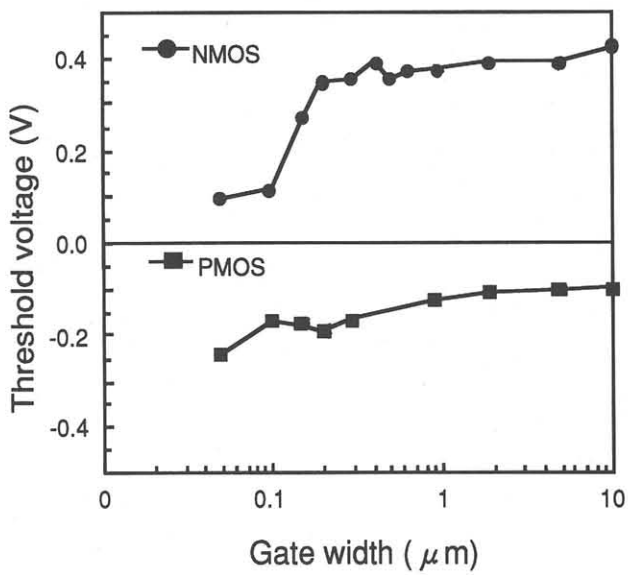

Fig. 8 Threshold voltage of 0.18 μm gate-length MOSFET vs. gate width with ON-LOCOS.