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Application of CVD SiO_2 Single Layer Films to Inter-Poly Dielectrics of Flash Memories

T. Kobayashi, M. Ushiyama, N. Miyamoto*, J. Yugami, H. Kume and K. Kimura

Central Research Laboratory, Hitachi, Ltd., Kokubunji, Tokyo 185, JAPAN
*Hitachi Device Engineering Co., Mobara, Chiba 297, JAPAN

In this paper, we first report the application of CVD SiO_2 single layer films to inter-poly dielectrics of flash memories to improve scalability and reliability. Leakage current analysis using a two-region model indicates that electric field enhancement at the pattern edges of the floating gates should be controlled to maintain the threshold voltage window margin because these films have Fowler-Nordheim-type conduction. Memory cells with 0.28 μm gates are operated using CVD SiO_2. Programming/erasing endurance can be dramatically improved compared to using conventional ONO films.

1. Background

Flash memories are promising candidates for future file memories of PDA. In these memories, $SiO_2/Si_3N_4/SiO_2$ composite (ONO) films are used as inter-poly dielectrics. However, the scaling of the memory cells poses three problems on the ONO films: (1) thinning limitation (~13 nm)[1], (2) high processing temperatures (>900°C), and (3) degradation of tunnel oxide due to Si_3N_4 stress[2]. To solve these problems, the CVD SiO_2 single layer films are applied to the inter-poly because of their good thickness controllability, low-temperature (750°C) processing, and low stress.

2. Experimental

Leakage current of CVD SiO_2 was measured by using capacitors with various edge lengths of the lower poly-Si patterns, as shown in Fig. 1. The CVD SiO_2 films, 15 nm thick, were deposited by pyrolyzing SiH_4 and N_2O at 750°C. Memory cells[3] were also fabricated to measure the programming/erasing characteristics. Constant current stress testing was performed using other MOS capacitors with the inter-poly dielectrics on poly-Si gates[2].

3. Results and discussion

We first studied the leakage current of CVD SiO_2 films in detail. Compared to the Poole-Frenkel conduction of ONO films, the leakage current of CVD SiO_2 films is the Fowler-Nordheim type; it increases significantly with edge length L of the lower poly-Si patterns when a positive bias is applied (Fig. 2). Because the slope of the edged pattern is smaller than that of the flat pattern, we consider that the leakage increase results from the electric field enhancement at the pattern edges of the lower poly-Si.

Next we will discuss leakage current of the CVD SiO_2 under the electric field enhancement. A two region model[4] (Fig. 3) is adopted to evaluate the electric field enhancement. In this model, the leakage is divided into two parts. In the flat area, S_1, the electric field across the SiO_2, E_1, is E_{ox}. At the pattern edge, S_2 (=L x W), the electric field is enhanced to XE_{ox}. Here, X and W are the field enhancement factor and its width, respectively. If the edge current is dominant, the measured leakage current can be written as

$$J/E^2=C(S_2/S)\exp(-B/XE_{ox}), \qquad (1)$$

where, C and B are constants related to the effective mass and the barrier height of the SiO_2, respectively. Comparing the F-N plots of the CVD SiO_2 on the flat pattern with those on the edged pattern, we can find X and S_2 from the slope and intercept. As shown in Fig. 4, the slope of the F-N plots is reduced to 0.63 for the edged pattern, which means that the field enhancement factor is 1.6. The field enhancement width is obtained by fitting J with the experimental results using various S_2/S values (Fig. 5). The best agreement between experiment and calculation is at S_2/S equal 1.2×10^{-3}. Since L is 43 cm, the field enhancement width is obtained as 1.1 nm. Considering the electric field enhancement, the calculated leakage current of the inter-poly in an actual memory cell increases more than two orders of magnitude (Fig. 6).

Next we will discuss memory cell characteristics under electric field enhancement. Figure 7 shows the threshold voltage shift of a memory cell when CVD SiO_2 is used as the inter-poly dielectrics. The calculations are performed from the charge balance between the injection to the floating gate through tunnel oxide and ejection through the inter-poly. Here, the calculated leakage current of CVD SiO_2 (Fig. 6) is used to estimate the ejection amount. The calculated results agree well (within 1 V) with the experimental results (Fig. 7). The shift saturates at 5 V, which is rather small compared to ONO films. Therefore, reducing the field enhancement, for example by rounding the pattern edges of the floating gate, is indispensable for improving the operation margin of memory cells.

Memory cells with CVD SiO_2 single layer films show high performance compared to those with conventional ONO films. Figure 8 shows the threshold voltage dependence on the gate length of the MOSFET. A minimum gate length of 0.28 μm is obtained with CVD SiO_2 because of the processing temperature reduction (900 to 750°C) of the inter-poly.

CVD SiO_2 films effectively improve programming/erasing endurance. Figure 9 shows the degradation in ejection time due to programming/erasing cycles. The start of degradation is delayed one order of magnitude by using CVD SiO_2. Figure 10 shows the gate voltage variance of MOS capacitors when a constant current stress (-10 mA/cm^2) is applied to the tunnel

oxide. The voltage variance due to electron trapping is reduced by using CVD SiO_2. These results indicate that the improvement in programming/erasing endurance results from less degradation in the tunnel oxide due to the low stress or low temperature processing of the inter-poly.

4. Conclusion

CVD SiO_2 single layer films are candidates for the inter-poly dielectrics of high-performance deep sub-micron flash memories. The electric field enhancement should be controlled to maintain threshold voltage window margin.

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6. References

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(2) M. Ushiyama, *et al.*, Proc. IEEE IRPS (1995) pp. 18.
(3) H. Kume, *et al.*, IEEE Tech. Dig. IEDM (1992) pp. 992.
(4) J. Yugami, *et al.*, Proc. IEEE ICMTS (1991) pp. 17.

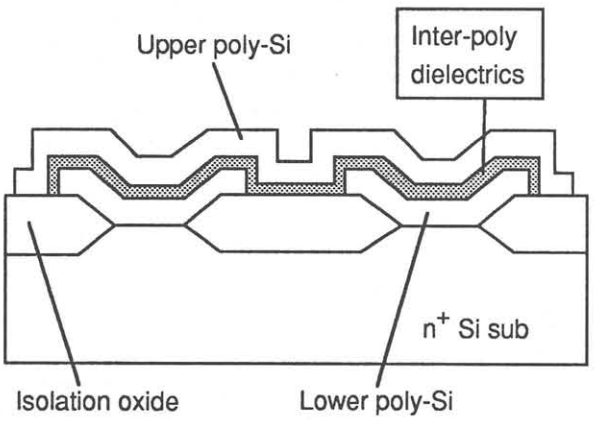

Fig. 1 Cross-sectional view of capacitor used to measure leakage current of CVD SiO_2 films.

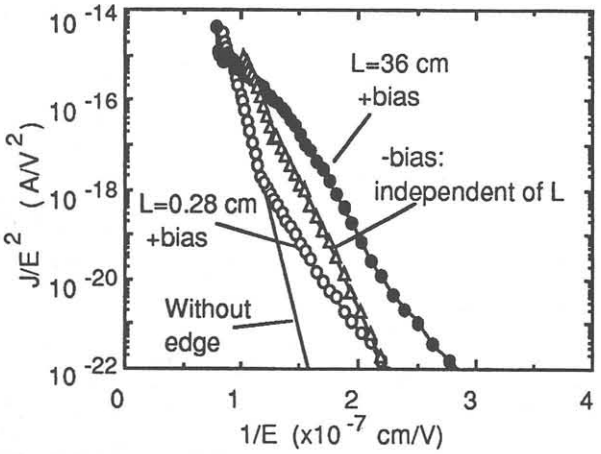

Fig. 2 F-N plots of CVD SiO_2 films deposited on various lower poly-Si patterns with different edge lengths L.

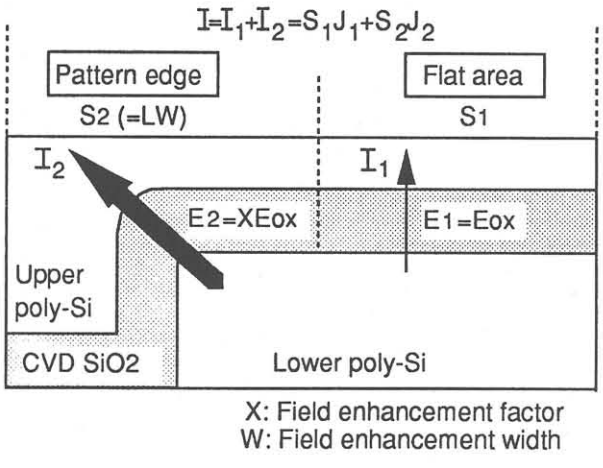

Fig. 3 Schematic diagram of leakage current of CVD SiO_2 films.

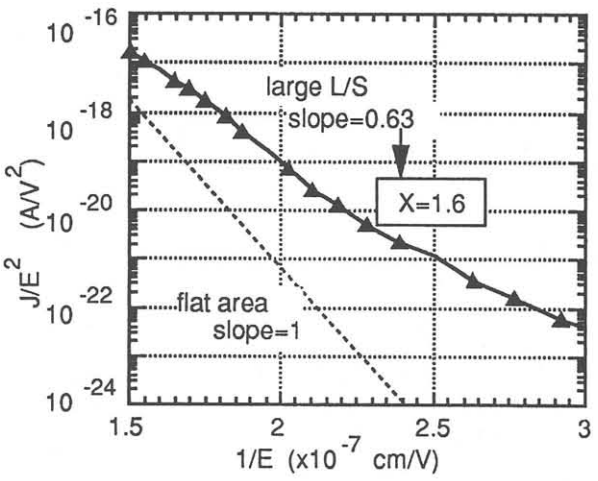

Fig. 4 Calculation of the field enhancement factor X.

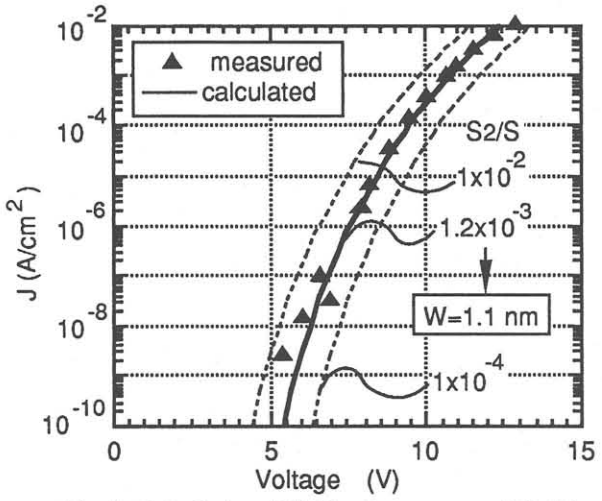

Fig. 5 Calculation of field enhancement width W.

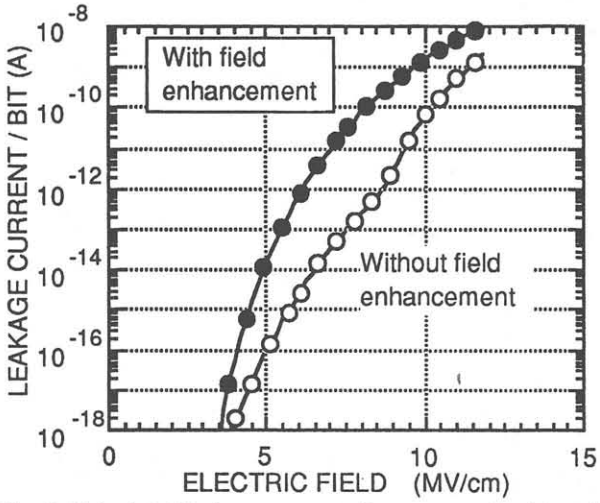

Fig. 6 Calculated leakage current of memory cell with and without consideration of field enhancement.

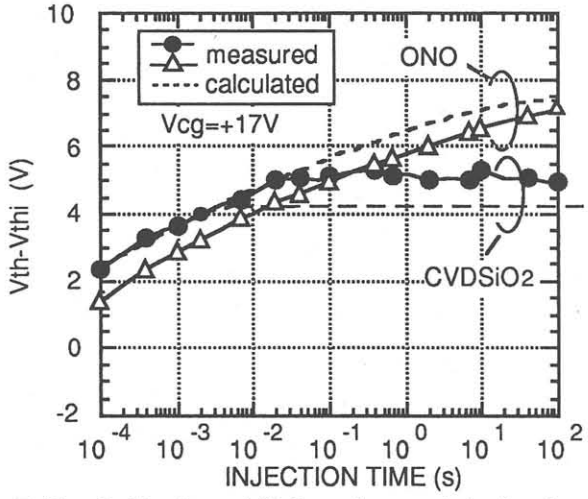

Fig. 7 Threshold voltage shift dependence on injection time.

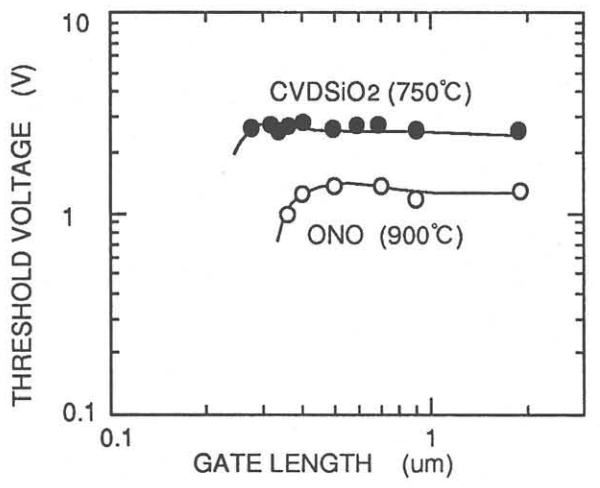

Fig. 8 Threshold voltage dependence on gate length. Gate electrodes are directly conected to the floating gates.

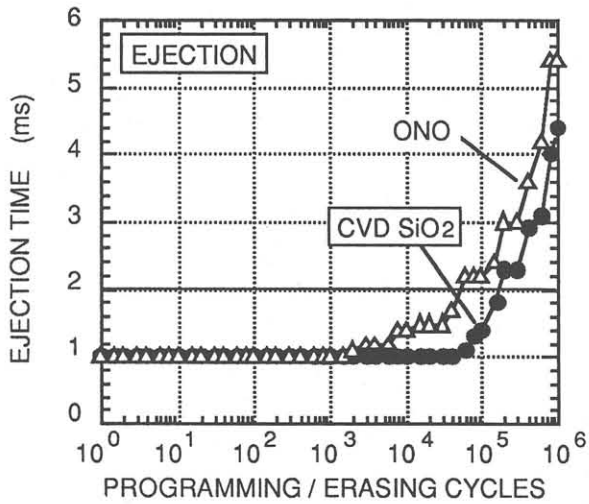

Fig. 9 Ejection time degradation due to P/E cycles.

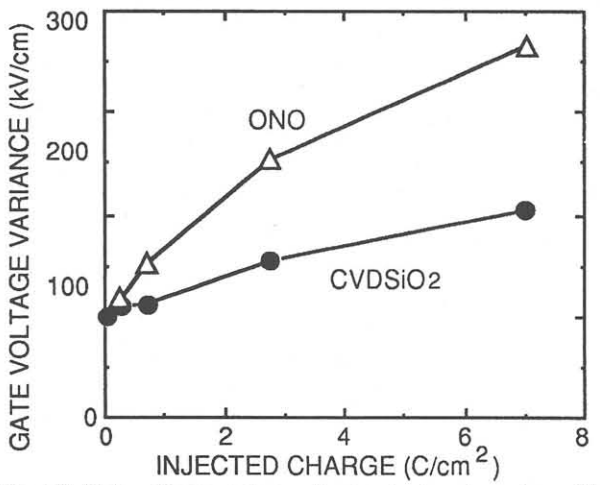

Fig. 10 Gate voltage variance due to electron trapping with constant current stress (-10 mA/cm^2).