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Developments in Consumables Used in the Chemical Mechanical Polishing of Dielectrics

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Developments in processing technology for logic components are driving the need for Chemical Mechanical Polishing (CMP) of both dielectrics and conductors. CMP remains the only planarization technique that provides a planar surface over distances of the order of the die size of advanced microprocessors (greater than 10mm on edge). Such global planarity is necessitated by very tight CD control needs in lithography and etching, stringer elimination in etching, and overall process simplification. Of these, the lithographic depth of focus requirement is the dominant issue due to the limited exposure latitude of the advanced deep UV (DUV) steppers, as shown in Table 1. Aggressive global planarization requirements driven by the increasing stepper field size and the limited depth of focus latitude fit the capabilities of the dielectric CMP process.

Table 1. Lithography trends

Min. Feature Size (micron)	Light Source	Lens NA	Depth of Focus (micron)	Field Size (mm)
1.0	G-line	0.35-0.4	~3	15
0.8	G-line	0.45-0.50	~2	17-20
0.5	I-line	0.55-0.6	~1	20-22
0.35	I-line (PSM?),	0.8	0.6	>20
	DUV	0.6	0.7	
0.25	DUV (PSM?)	0.75 (?)	0.4 (?)	>25(?)

Traditionally, various forms of SiO_2 such as BPSG, plasma enhanced CVD oxides, and TEOS based oxides have been polished using a consumable set combination of fumed silica slurry stabilized by KOH and a double pad of cast and filled polyurethane with a fibrous soft lower pad. This combination has provided acceptable removal rates with less than desirable non-uniformities. Figure 1 shows the removal rate and non-uniformity from such a consumable set for thermal oxide sheet film wafers.

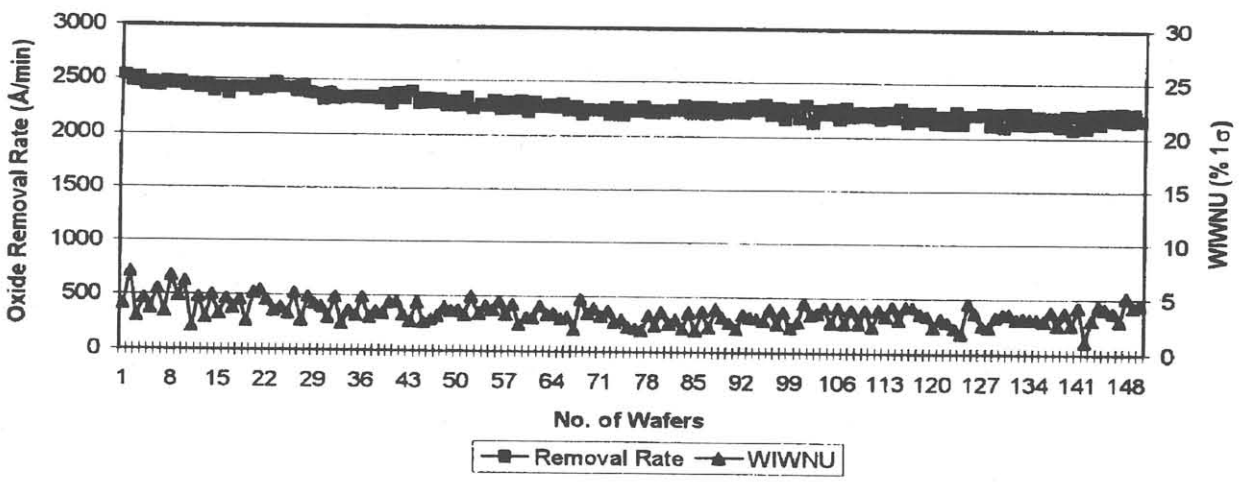

Figure 1. Typical polishing results using KOH slurry and stacked pad

More recently, however, a new set of requirements has been imposed on the dielectric polishing process. These include (a) the use of fluorinated oxides in order to achieve reduced dielectric constants, (b) the use of integrated high density plasma and conventional plasma oxide stacks for better gap filling characteristics, (c) spun on materials for reducing metallization stresses and lowering the dielectric constant, and (d) enhanced sensitivity to mobile ions, particularly for the poly-level dielectric polishing, that precludes K and Na ions from the polishing slurry. When more conventional polishing requirements such as stable and high removal rates, very low within-wafer and wafer-to-wafer non-uniformity, better planarity over longer range, and elimination of scratches are added on to the list stated above, the consumable set becomes a critical piece for successful integration of the CMP process.

New developments in the slurry to handle these requirements include the development of the ammonia stabilized slurries to replace the KOH based slurry in order to address the mobile ion issue (see Figure 2), increased pH to increase removal rate while still controlling silica dissolution, and better size control of the fumed silica particle aggregate have imparted better control to the slurries (Table 2). Direct polishing performance improvements resulting from the use of ammonia stabilized slurry materials include improved cleanability of the wafer surface and smoother post-polish oxide surface roughness.[1)] For pads, surface treatments or "pad conditioning" techniques have been widely implemented to maintain consistent surface conditions.[2)] New pad materials and composites are also being developed to address the issues of pad deformation and polish rate control.

Table 2. Properties of Slurries

	SC112	Semi-sperse 25
Buffering Agent	KOH	KOH
pH	10.2-10.35	10.9-11.2
Aggregate particle size	100nm	100nm
Removal rate	137.4 nm/min	226.6 nm/min
Within-wafer non-uniformity	4.4% (1 sigma)	3.5% (1 sigma)

Data: Rippey Corp.

The impact of these developments on device integration has been significant. Interlevel dielectrics that use composite or fluorinated oxides need to take special precaution not to expose multiple oxide types simultaneously to the polishing process. Post-polish cleaning techniques to remove pad debris and slurry residue have changed significantly to address different slurry compositions.[3)] Defect reduction as a result of the CMP process with better controlled consumables has been well quantified.

This paper will address the implications of the device requirements on dielectric polish and compare it to the new directions in consumables. Areas of deficiencies in the consumables from a logic device perspective will be highlighted.

References

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