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Impact of Negative-Bias Temperature Instability on the Lifetime of Single-Gate CMOS Structures with Ultrathin(4-6 nm)Gate Oxides

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The lifetime of ultrathin gate oxides at low-field stresses has been studied on the basis of negative-bias temperature instability (NBTI) up to 5,000 hours for the 4.2-to-30-nm-thick oxides of MOS systems. The derived lifetime and maximum acceptable operating voltage are strongly dependent on the reliability specification. Since NBTI-induced interface traps increase with decreasing oxide thickness (T_{ox}) as T_{ox}^{-1}, this instability becomes an important factor limiting the lifetime of single-gate CMOS structures with ultrathin oxides.

1. Introduction

Negative-bias temperature instability (NBTI) can be a major threat to the long-term stability of p-channel MOS devices with n+ poly-Si gates,[1] because the polarity of the gate bias is negative. The increase in positive fixed oxide charge and in donor-like interface-trap density (D_{it}) in the lower half of the Si bandgap[2] causes an unwanted negative threshold voltage shift. However, for CMOS devices with thick gate oxides (> 10 nm), NBTI-induced interfacial charges are not the main factors determining the device lifetime. Recently, we observed that, for MOS devices with ultrathin oxides, the induced interface-trap density increases with decreasing oxide thickness (T_{ox}) as T_{ox}^{-1}, whereas the induced fixed oxide charge density was found to have no thickness dependence.[3] This T_{ox}^{-1} dependence of interface-trap generation implies that the NBTI becomes more severe so as to limit the device lifetime for ultrathin oxides. The lifetime is commonly estimated by high-field accelerated time-dependent dielectric breakdown (TDDB) lifetests. However, there have been very few reports about the long-term reliability under low-field stress conditions. In this paper, we show that the results of NBT aging up to 5,000 hours for 4.2-to-30-nm-thick oxides can be used to project the lifetime, the maximum acceptable operating voltage in nanometer range oxides.

2. Experimental

Test devices were n+ poly-Si gate MOS capacitors with 4.2-to-30-nm-thick oxides, fabricated on p-type (100) Si wafers by a damageless wet process, rather than MOSFETs fabricated on n-type substrates. This is because the contribution of fixed oxide charges and interface traps can be separately analyzed and the NBTI is independent of the substrate polarity.[1] Furthermore, with p-type samples, the D_{it} distribution in the lower half of the Si bandgap can be measured by the conductance technique, which is time consuming but very reliable even in ultrathin oxides.[3]

Negative-bias temperature aging of these capacitors was carried out by applying moderate oxide fields varied from −1.6 to −5 MV/cm in accumulation at 150−290 °C. The maximum aging time was 5,000 hours. The midgap voltage shift (ΔV_{MG}), from which the surface density of induced fixed oxide charges (ΔN_f) is estimated as $C_{ox}|\Delta V_{MG}|$ / e, and the increase in interface-trap density (ΔD_{it}) were evaluated at the scheduled aging periods at room temperature. To characterize the D_{it} generation, we use the integrated interface-trap density (N_{it}).[3]

3. Results and Discussion

3.1 Acceleration Equation

Figure 1 shows the time evolution of the ΔN_{it} and ΔN_f typically measured for 6.2-nm- and 21.0-nm-thick oxide MOS capacitors subjected to NBT aging tests. The induced N_{it} is greater for the 6.2-nm-thick oxide than for the 21.0-nm-thick oxide.

As shown in Figs. 2(a) and (b),[3] the various experimentally observed dependencies of N_{it} and N_f generation for ultra-thin oxides can be written by the simple empirical expressions (hereafter, Δ is omitted)

$$N_{it}(E_{ox}, T_{ox}, T, t) = B\, E_{ox}^{3/2}\, t^{1/4} \exp(-E_A^{it}/k_BT) / T_{ox}, \quad (1)$$

$$N_f(E_{ox}, T_{ox}, T, t) = C\, E_{ox}^{3/2}\, t^{0.14} \exp(-E_A^{f}/k_BT), \quad (2)$$

with

$$B = 9.018 \times 10^{-4}\ (\mathrm{cm})^{-1}(\mathrm{cm/V})^{3/2}(\mathrm{kh})^{-1/4},\ E_A^{it} = 0.20\ \mathrm{eV},$$

$$C = 4.899 \times 10^{2}(\mathrm{cm})^{-2}(\mathrm{cm/V})^{3/2}(\mathrm{kh})^{-0.14},\ E_A^{f} = 0.15\ \mathrm{eV}.$$

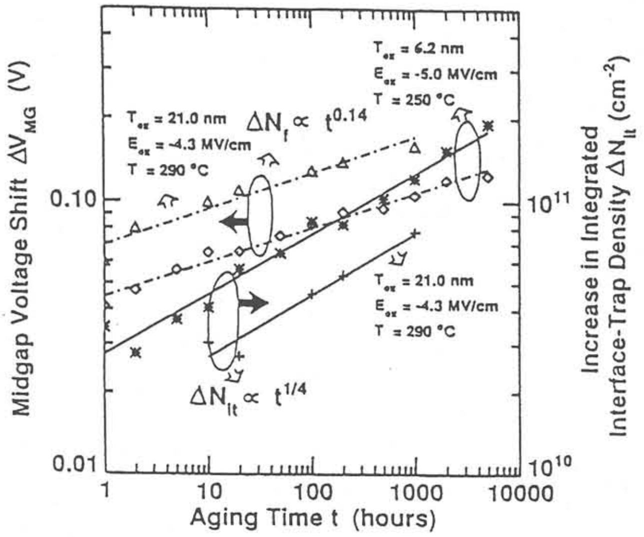

Fig. 1 The time evolution of induced integrated interface-trap densities (ΔN_{it}) and the change in midgap voltage (ΔV_{MG}), which is proportional to induced fixed oxide charge densities (ΔN_f), measured for 6.2-nm- and 21.0-nm-thick oxide MOS capacitors subjected to negative BT aging tests. The main part of ΔV_{FB} for the ultrathin oxide is due to the ΔN_{it} whereas ΔV_{FB} for the thick oxide is mostly due to the ΔN_f.

Here, N_{it} and N_f are the surface densities of generated interface traps and fixed oxide charges in cm^{-2} units, E_{ox} is the applied oxide field in V/cm units, t is the aging time in kilo hours, k_BT is the thermal voltage at the aging temperature in eV units, and T_{ox} is the oxide thickness in cm. N_{it} and N_f obtained from Eqs. (1) and (2) differ from the measured values by 10% at most.

The inverse proportionality to oxide thickness and the fractional power law dependence to aging time for the N_{it} generation in Eq. (1) can be explained by a generalized diffusion-reaction chemistry between hydrogenated trivalent silicon and the neutral-diffusing (atomic or molecular) hydrogen with an absorbing wall at the gate electrode-oxide interface.[4)]

3.2 The Lifetime Projection Method

The lifetime τ_{NBTI} is defined as the maximum time when NBTI will cause a specified flatband voltage shift (ΔV_{FB}) under operation with specified operating voltages at 85°C. Here, ΔV_{FB} is expressed by

$$\Delta V_{FB} = -\{\Delta Q_f + \Delta Q_{it}(\Psi_s=0)\}/C_{ox} \text{ (for p-Si MOSCAP)}, \quad (3)$$

where $\Delta Q_f = eN_f$ and $\Delta Q_{it} = eN_{it}$ are changes in fixed oxide charges and interface-trap charges from the initial state, $Q_{it}(\Psi_s = 0)$ is the interface-trap charge at the flatband, and C_{ox} is the oxide capacitance per unit area. The threshold voltage shift of p-channel MOSFETs can be approximated by ΔV_{FB} of p-type Si MOS capacitors as follows:[2)]

$$\Delta V_{Th}^{\text{p-ch.MOSFET}} \cong \Delta V_{FB}^{\text{p-SiMOSCAP}}. \quad (4)$$

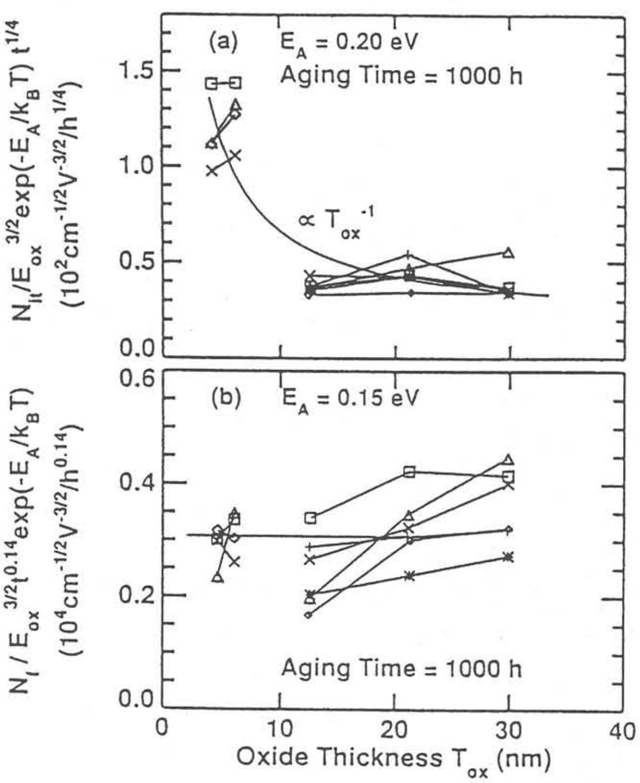

Fig. 2 (a) Oxide thickness (T_{ox}) dependence of the rate of change of integrated interface-trap densities $\Delta N_{it}/\Delta t^{1/4}$ (Δ is omitted in the ordinate) normalized by the empirical equation $E_{ox}^{3/2}\exp(-0.20\text{eV}/k_BT)$ with the T_{ox}^{-1}-model fitting. It turns out that the normalized ΔN_{it} is always inversely proportional to T_{ox}. (b) T_{ox}-dependence of the rate of change of fixed oxide charge densities $\Delta N_f/\Delta t^{0.14}$ (Δ is omitted in the ordinate) normalized by the empirical equation $E_{ox}^{3/2}\exp(-0.15\text{ eV}/k_BT)$. It turns out that the normalized ΔN_f is independent of T_{ox}.

Solving Eqs. (1) and (2) for t with specified voltage shifts (ΔV_{it} and ΔV_{MG}), we obtain the approximate lifetime formula

$$\tau_{it} \propto T_{ox}^{6}\, V_{ox}^{-6}\, (\Delta V_{it})^4 \exp(4\, E_A^{it}/k_BT), \quad (5)$$

and $$\tau_f \propto T_{ox}^{3.57}\, V_{ox}^{-10.7}\, (\Delta V_{MG})^{7.14} \exp(7.14\, E_A^{f}/k_BT). \quad (6)$$

These analytical equations approximate the lifetime for ultrathin and thick oxides, respectively.

By combining acceleration Eqs. (1) and (2) with (3) with a specified NBTI degradation criterion (e.g., $|\Delta V_{FB}(85°C)| \leq$ 10-or 100-mV, etc.), the lifetime can numerically be projected as a function of oxide thickness, as shown in Fig. 3.

In a similar way, Fig. 4 shows the T_{ox} dependence of the maximum acceptable oxide voltage V_{ox_limit} with which 10 year operation at 85°C will cause the specified changes in V_{FB} (solid lines) due to NBTI. In Figs. 3 and 4, the projected curves with the specified ΔV_{FB} are compared to the curves projected from temperature-accelerated intrinsic TDDB lifetime tests

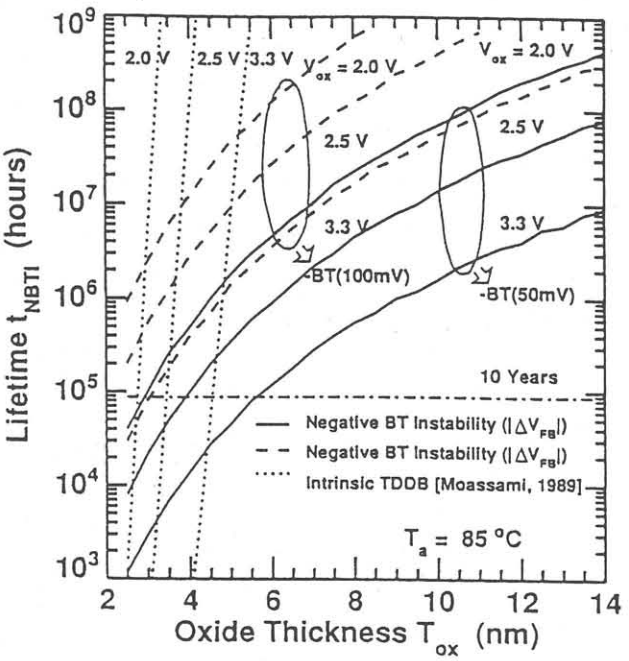

Fig. 3 Oxide thickness dependence of lifetime projected by empirical equations for NBTI with specified V_{FB} change under various operating voltages (2.0, 2.5, and 3.3V) at 85°C. These lifetime curves are compared with those projected from intrinsic TDDB.[5]

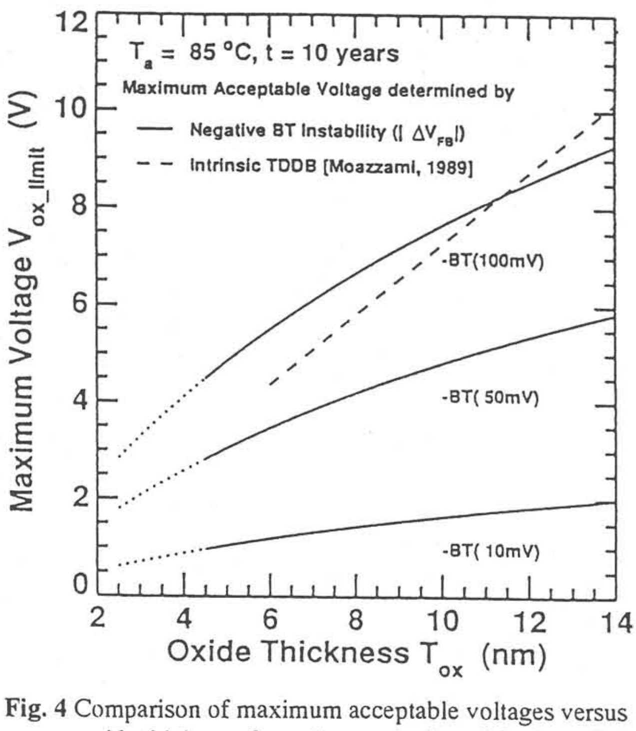

Fig. 4 Comparison of maximum acceptable voltages versus oxide thickness from the standpoint of the low-field NBTI and intrinsic TDDB[5] at 85°C. TDDB data is extrapolated to the ultrathin region, where its validity awaits further study.

on dry oxides[5] (broken and dashed lines in Figs. 3 and 4, respectively). These figures show that theNB-TI-limiting lifetime and maximum acceptable operating voltage are strongly dependent on the reliability specification and that the voltage inducing several-decades-mV change in V_{FB} may be significantly lower than that projected from a given TDDB specification.[5]

4. Conclusion

The lifetime of ultrathin gate oxided at low-field stress conditions has been studied on the basis of empirical acceleration equations for NBTI. The equations show the N_{it} generation becomes a dominant contributor to ΔV_{FB} at the same aging condition with decreasing oxide thickness, since the NBTI-induced N_f remains constant irrespective of oxide thickness. The derived lifetime and maximum acceptable operating voltage were compared to reported results of high-field TDDB lifetests, which are widely used to characterize ultrathin gate oxide reliability nowadays, and shown to be more sensitive to the reliability specification. The observed T_{ox}^{-1} dependence of N_{it} generation and the fact that NBTI occurs under conditions where there is no measurable current through oxides imply that the NBTI becomes an important factor limiting the lifetime of single-gate CMOS structures with ultrathin gate oxides.

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