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Thermal Budget for Fabricating A Dual Gate Deep-Submicron CMOS with Thin Pure Gate Oxide

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Abstract

We studied the diffusion phenomenon of impurities in a dual polysilicon gate, and clarified the thermal budget for suppressing gate depletion and impurity penetration through the gate oxide. According to our study, the thermal budget for dual gate deep-submicron CMOS is wide enough using pure SiO_2.

1. Introduction

Deep submicron devices require surface channels to suppress short channel effects, and a p^+-polysilicon gate should be used for pMOSFETs while an n^+-polysilicon gate is used for nMOSFETs. The thermal processing conditions for both n^+- and p^+-polysilicon gates should be determined, ensuring a flat impurity profile in the polysilicon to suppress gate depletion, and alleviating impurity penetration through the thin gate oxide. To relax the thermal budget, an oxynitride film has been investigated as an alternative. However, it should be clarified how a thin pure SiO_2 can be used, satisfying the above requirements. In this paper, we have modeled impurity diffusion in polysilicon and gate oxide, and clarified the thermal budget for fabricating a dual gate with thin gate oxide for 0.1 μm CMOS generation.

2. Experiment

In order to investigate the diffusion mechanism in a polysilicon gate, Si (100) substrates were oxidized to produce a 4- nm thick silicon dioxide (SiO_2) layer, and a 0.18 μm thick polysilicon layer was deposited by low-pressure chemical vapor deposition at 620°C and 30 Pa. BF_2 was ion implanted at 20 keV with 5 x 10^{15} cm^{-2} for p^+-polysilicon, and As was ion implanted at 30 keV with 5 x 10^{15} cm^{-2} for n^+-polysilicon gate. A 100-nm thick SiO_2 layer was deposited at 420°C by chemical vapor deposition to prevent impurity out diffusion, and the substrates were subjected to various annealing. After removing the top SiO_2 layer, we evaluated the impurity profile in polysilicon using Secondary Ion Mass Spectrometry (SIMS).

3. Results and Discussion

We found that both the B and As profiles in polysilicon can be divided into two regions, one is the region where the alloy is formed and the impurity is immobile [1], and the other is the region that has a constant surface concentration, N_0 (Fig. 1). N_0 increases with increasing annealing temperature for B and is almost constant for As (Fig. 2), and both N_0 values were identified as

$$N_0(B) = 8.91 \times 10^{21} \exp\left[-\frac{0.38\ (eV)}{k_B T}\right] cm^{-3}$$
$$N_0(As) = 2.50 \times 10^{21}\ cm^{-3} \quad . \qquad (1)$$

Using the above findings, we derived an analytical model for the impurity diffusion profile in the region II of Fig. 1:

$$N(x,t) = N_0 - \sum_{k=0}^{\infty} \frac{4N_0}{(1+2k)\pi} \exp\left(-\frac{t}{\tau_k}\right) \sin(\lambda_k x), \qquad (2)$$

where

$$\lambda_k = \frac{(1+2k)\pi}{2d} : \tau_k = \frac{1}{\lambda_k^2 D_{poly}}. \qquad (3)$$

When enough time passes for impurities to reach the polysilicon/gate oxide interface, only the term associated with k = 0 dominates the summation in Eq. 2, and the profile reduces to

$$N(x,t) = N_0\left[1 - \frac{4}{\pi}\exp\left(-\frac{t}{\tau_0}\right)\sin(\lambda_0 x)\right]. \qquad (4)$$

From Eq. 3,

$$\tau_0 = \frac{4d^2}{\pi^2 D_{poly}}. \qquad (5)$$

The analytical model of Eq. 2 agrees well with the experimental data for various conditions using a diffusion coefficient as a fitting parameter as shown by the solid lines in Fig. 1. We performed a similar analysis at different temperatures, and obtained diffusion coefficients in polysilicon, D_{poly}, for B and As:

$$D_{poly}(B) = 2.33 \times 10^3 \exp\left[-\frac{3.49\,(eV)}{k_B T}\right] cm^2/s$$

$$D_{poly}(As) = 8.80 \times 10^3 \exp\left[-\frac{3.65\,(eV)}{k_B T}\right] cm^2/s \quad . \quad (6)$$

These are lager than the intrinsic diffusion coefficients in silicon [2] by more than three orders (Fig. 3). Note that $D_{poly}(B)$ is almost the same as $D_{poly}(As)$, and hence the thermal condition for flattening the impurity profile in polysilicon is almost the same for n^+- and p^+-polysilicon gates.

Using Eq. 4, we can robustly define the flatness of the impurity profile in polysilicon as $N(d)/N_0 = r$ (we used $r = 0.9$), which leads to the critical time t_1 to make the impurity profile flat as

$$t_1 = \tau_0 \ln\left[\frac{4}{(1-r)\pi}\right] . \quad (7)$$

The upper limit of the annealing time is determined by impurity penetration into a silicon substrate through the gate oxide. We have already modeled the critical time, t_2, as [3, 4]

$$t_2 = \frac{t_{Ox}^2}{4D_{SiO_2}} \frac{1}{\left[\mathrm{erfc}^{-1}\left(\frac{m+\gamma}{2\gamma}\frac{N_C}{N_0}\right)\right]^2} , \quad (8)$$

where

$$\gamma = \sqrt{\frac{D_{SiO_2}}{D_{Si}}} . \quad (9)$$

t_{Ox} is the gate oxide thickness, D_{SiO2} is the diffusion coefficient of impurity in SiO_2, m is the segregation coefficient of impurity in the polysilicon or silicon/SiO_2 system and is 0.357 for B and around 50 for As [5], N_C is the doping concentration at the interface in the silicon, and we set N_0/N_C to 10000 to evaluate impurity penetration.

From the above results, we obtained the thermal budget for a dual gate CMOS with a t_{Ox} of 3 nm as $t_1 < t < t_2$ (Fig. 4). t_{Ox} is limited to 3 nm by tunneling, and the thickness is expected for 0.1 μm CMOS generation. It is clear from Eq. 8 that t_2 is dominantly determined by the diffusion coefficient in SiO_2. Since the line up for D_{SiO2} is $D_{SiO2}(BF_2) > D_{SiO2}(As) > D_{SiO2}(B)$ as shown in Fig. 3, and hence the line up for t_2 of $t_2(BF_2) < t_2(As) < t_2(B)$ is expected. However, $t_2(As)$ is shorter than $t_2(B)$, which is due to the much larger segregation coefficient of As than that of B. Therefore, we can focus only on p^+-polysilicon to determine the thermal budget of dual gate CMOS processes. Although the allowable annealing time exists at any temperature, the annealing temperature should be as high as possible to decrease sheet resistance.

The minimum annealing time that modern RTA equipment can ensure is around 5 s. Therefore, we cannot use a temperature if the corresponding t_2 is less than 5 s. Furthermore, if t_1 is close to t_2, there is little process margin. The maximum temperature should be chosen to adhere the following condition:

$$t_2 >> 5 \text{ s and } t_1 << t_2 . \quad (10)$$

From the criterion and from Fig. 4, BF_2 ion implantation suffers restricted thermal budget, and t_2 is only 20 s for 1000°C. B ion implantation provides t_2 of 200 s for 1000°C, which is wide enough to use in the practical thermal processing.

4. Conclusion

We have modeled impurity profiles in polysilicon and oxide, and clarified the thermal budget for fabricating dual gates with thin gate oxide. The thermal budget for n^+-polysilicon gate is always wider than that for p^+-polysilicon gate. The p^+-polysilicon gate doped with B instead of BF_2 provides a wide thermal budget enough to use annealing temperature of more than 1000°C. We can fabricate the dual gate with a 3-nm-thick pure gate oxide, ensuring a uniform impurity profile in polysilicon and alleviating impurity penetration into the substrate. Consequently, pure SiO_2 can keep its position as gate insulator at least 0.1 μm CMOS generation without introducing exotic gate insulator such as oxynitride.

References

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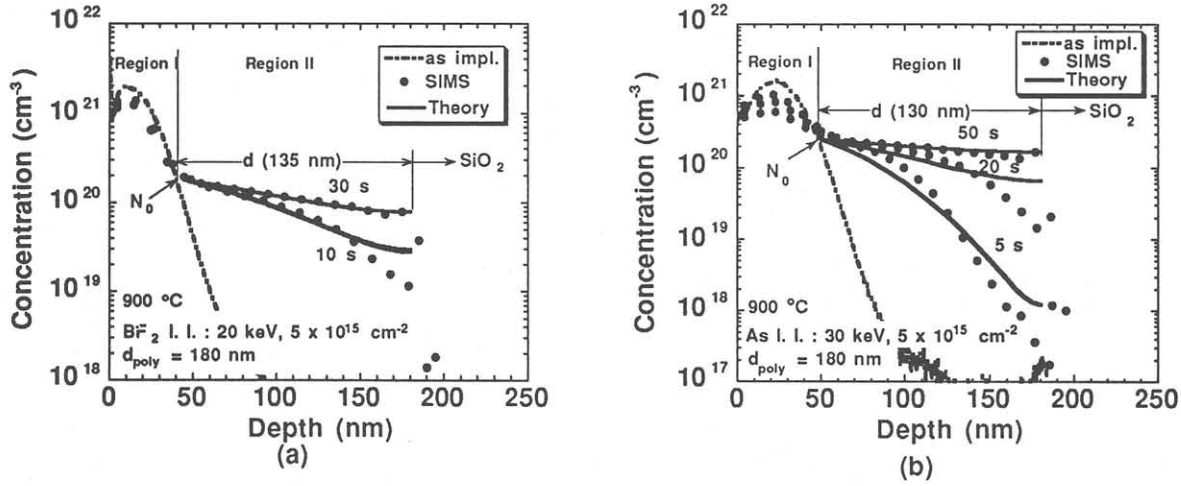

Fig. 1. Comparison between theoretical and experimental impurity profiles in polysilicon gate using a diffusion coefficient as a fitting parameter: (a) B; (b) As.

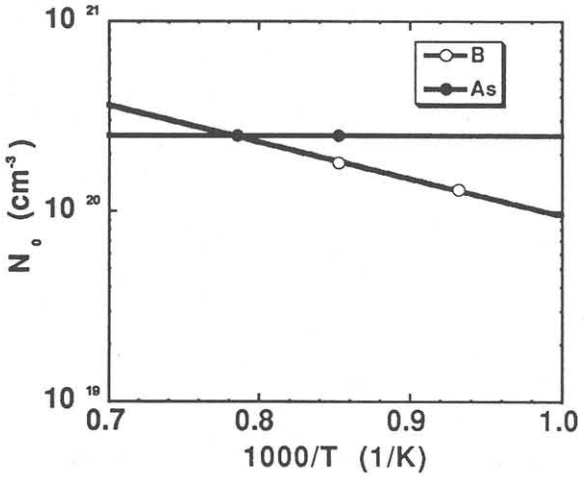

Fig. 2. Dependence of constant surface concentration N_0 on temperature.

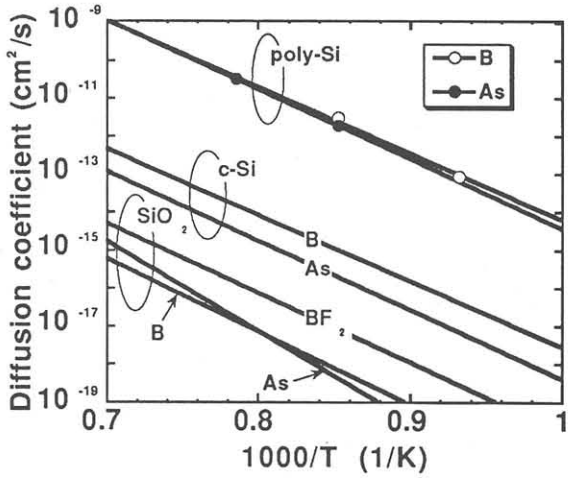

Fig. 3. Diffusion coefficient of B and As in polysilicon. Those in crystal Si and SiO_2 are also indicated.

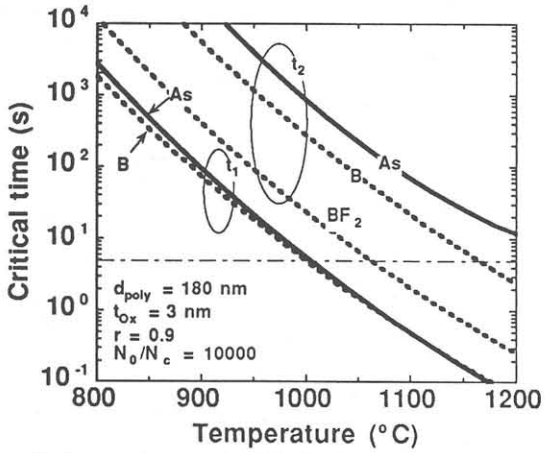

Fig. 4. Dependence of critical times on temperature. t_1 is the critical time for impurity profile in polysilicon to be flat, and t_2 is the critical time for impurity not to penetrate 3-nm-thick gate oxide.