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New Dielectric Breakdown Model of Local Wearout in Ultra Thin Silicon Dioxides

Kenji OKADA and Satoko KAWASAKI*,†

Micro Computer Division, Matsushita Electronics Corp.
Nagaokakyo, Kyoto 617, Japan
**Semiconductor Research Center, Matsushita Electric Ind. Co.,Ltd.*
3-1-1, Yagumo-Nakamachi, Moriguchi, Osaka 570, Japan

In the ultra thin oxides, the "B mode Stress Induced Leakage Current" (B mode SILC) has been observed. In this paper, the "B mode shift", which triggers the B mode SILC, is investigated and a new dielectric breakdown process model, the Four Stage Model, consisting of two - uniform and local - wearout modes is proposed. Based on this model, the contributions of the interface quality and the "bulk" oxide quality to the reliability are clarified.

1. Introduction

Advanced Si MOS LSI requires the ultra thin gate oxides (<5nm). It is well known that a Stress Induced Leakage Current, SILC, can be observed in the thin oxide region(<10nm)[1]. In the ultra thin oxide region, we have already reported a new mode of SILC (B mode SILC) for the first time[2]. The B mode SILC is clearly different from the already reported mode (A mode SILC) in its dependence on the temperature and the gate area. Recently after we reported the B mode SILC, quite a same phenomenon was reported[3]. In this paper, the "B mode shift" which triggers the B mode SILC is studied and a new breakdown process model in the ultra thin oxides is proposed, which is referred to as the Four Stage Model. Based on this new model, the contributions of the interface quality and the "bulk" oxide quality to the dielectric breakdown are clarified.

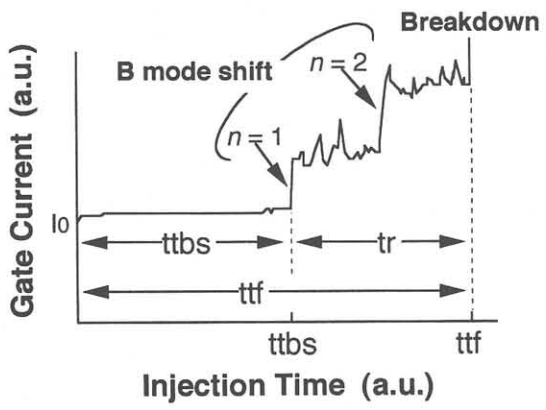

Fig. 1 Typical time dependence of the gate current for a 4nm-thick oxide under constant-voltage Fowler-Nordheim stress. The number of B mode shift is indicated by *n*.
Definitions of ttbs, tr and ttf are also shown.

2. Experimental

MOS capacitors with 4nm-thick gate oxides and n+ polycrystalline silicon gate electrodes were fabricated on CZ-p type Si (100) substrates. Various electrical characterizations including I-V and I-t measurements were performed on these samples under the accumulation region of the substrate silicon. The SiO_2/Si interface roughness was analyzed by the cross-sectional transmission electron microscopy (XTEM). From the XTEM photographs, root mean square of roughness, Δ_{RMS}, was determined.

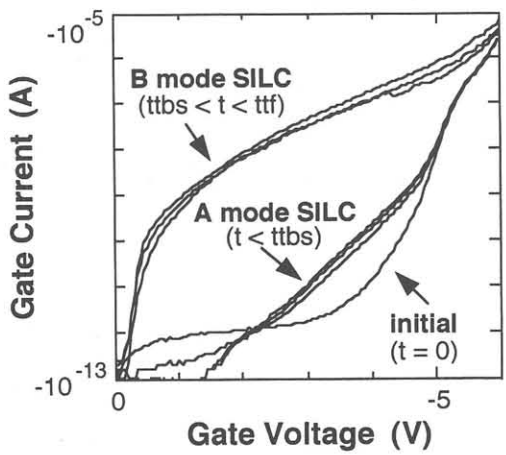

Fig. 2 Typical current-voltage characteristics of a MOS capacitor with 4nm-thick oxide film after repeated constant voltage F-N stresses.

† present address : *Kyoto Research Laboratory, Matsushita Electronics Corp., Minami-ku, Kyoto 601, Japan*

3. Results and Discussions

A typical time dependence of the gate current for a 4nm-thick oxide film under constant voltage Fowler-Nordheim (F-N) stress is shown in Fig.1. It is clear that a few B mode shifts are observed as abrupt shifts of the gate current (multi step B mode shift). The number of B mode shift is indicated by *n*. After the 1st B mode shift, the B mode SILC can be observed in I-V curve as shown in Fig.2. Fig.3 shows the relationship between the B mode SILC at the gate voltage of -4V and the number of B mode shift, *n*, taken for different samples. The linear dependence of the B mode SILC on *n* is clearly seen and the contribution from each B mode shift to the B mode SILC is almost constant (~0.1μA). This implies that the multi step B mode shift is nothing but a combination of single step B mode shifts which originate from unique physical process occurring at different times and different spots as shown by inset of Fig.3.

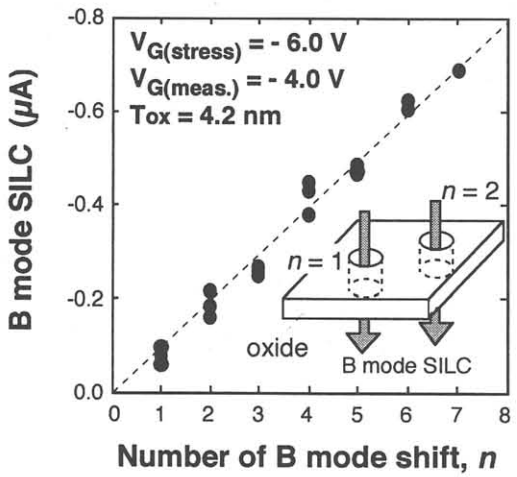

Fig. 3 The B mode SILC as a function of the number of B mode shift, *n*.

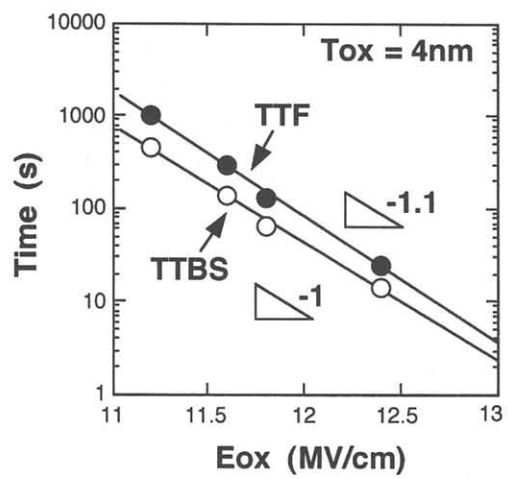

Fig. 4 The electric field dependence of TTF and TTBS.

Next, we will show that the conventional Two Stage Model (TSM)[4] cannot explain the dielectric breakdown of the ultra thin oxides but that the local wearout due to the B mode SILC plays the key role. It has been well known that the dielectric breakdown process for thicker oxides is explained by the TSM consisting of the buildup stage and the runaway stage[4]. Namely, the breakdown takes place after experiencing the uniform wearout over the entire oxide area. To see the validity of the TSM in the ultra thin oxides (Tox=4nm), following experiments were performed.

As the parameters of the occurrence of the B mode shift and the dielectric breakdown, three new parameters were defined, *i.e.*, Time To Failure (TTF), Time To the first B mode Shift (TTBS) and Residual Time to breakdown (TR). The definitions of I_0 (initial gate current), ttf, ttbs and tr are shown in Fig.1. (ttf = ttbs + tr) Using the Weibull plots of ttf, ttbs and tr, 50% level of cumulative events, TTF, TTBS and TR were calculated, respectively.

The TTBS depends on the stress field which is clearly

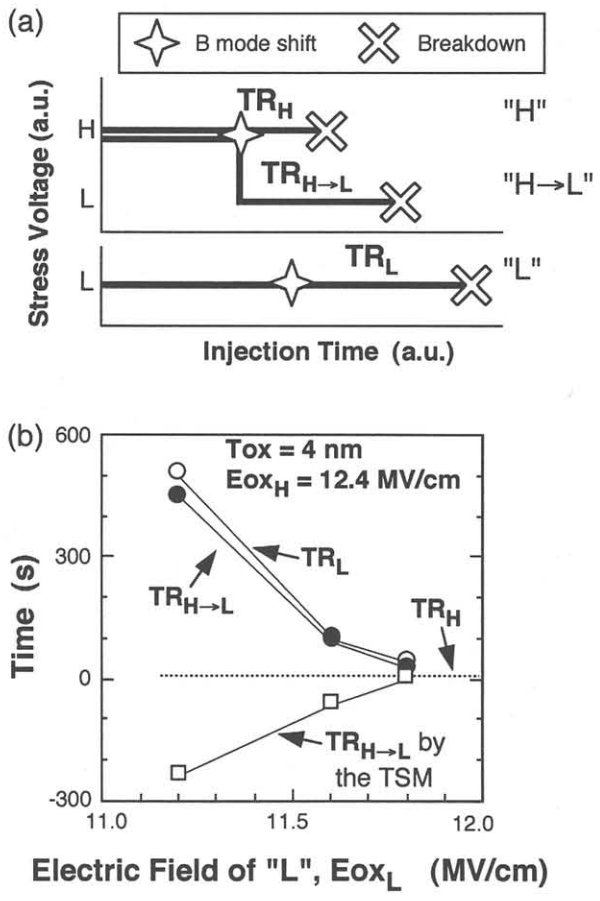

Fig. 5 (a) The definitions of three stress patterns "H", "H→L" and "L" ; and corresponding residual times to breakdown, TR_H, $TR_{H\to L}$ and TR_L, respectively.
(b) Experimental $TR_{H\to L}$ (●), TR_L (○) are compared with the $TR_{H\to L}$ calculated by the Two Stage Model(TSM) (□). The level of TR_H is also shown.

shown in Fig.4 for 4nm-thick oxides. It should be noted that the slope (the field acceleration factor) of TTF is slightly larger than that of TTBS.

Based on these results, three patterns of stress switching measurements were performed as shown in Fig.5(a). In the stress pattern "H" (or "L"), constant high (or low) electric field was applied up to breakdown to obtain TR_H (or TR_L). In the stress pattern "H→L", the stress was "switched" from the high field "H" to the low field "L" immediately after the first B mode shift to obtain $TR_{H\to L}$. If the TSM are applicable, $TR_{H\to L}$ should be expressed as follows;

$$TR_{H\to L} = TTF_L - TTBS_H \times K \qquad (1)$$

where TTF of stress pattern "H" and "L" correspond to TTF_H and TTF_L, respectively and TTBS of stress pattern "H" corresponds to $TTBS_H$ and K is a constant equal to TTF_L / TTF_H. Fig.5(b) shows the experimental TR_H, TR_L and $TR_{H\to L}$. (electric field of "H" : Eox_H=12.4 MV/cm, electric field of "L" : Eox_L=11.2, 11.6, 11.8 MV/cm) In Fig.5(b), calculated $TR_{H\to L}$ by the TSM is also plotted. It is clear that $TR_{H\to L}$ calculated by the TSM cannot explain the experimental result $TR_{H\to L}$. Rather, $TR_{H\to L}$ shows a dependence similar to TR_L. Hence, residual time from the first B mode shift to the breakdown, TR, does not depend on the stress condition prior to the B mode shift but depends only on the stress condition after the B mode shift. This implies that the breakdown process in the ultra thin oxides can be divided into two reactions, *i.e.*, the B mode shift and the "complete breakdown", and that they are expressed by TTBS and TR, respectively. Herein, we propose a new breakdown process model, the Four Stage Model (FSM); (1) the uniform wearout results in the B mode shift (partial breakdown) which triggers the B mode SILC at a local spot and; (2) the local wearout at the local spot due to the B mode SILC leads to the complete breakdown.

Fig.6(a) and (b) show the SiO_2/Si interface roughness dependence of TR and TTBS, respectively. The rougher the interface becomes, the shorter both TTBS and TR become. TR depends more on the roughness compared to TTBS. Moreover, when the POA (post oxidation anneal in N_2) is performed at 800°C, only TTBS is increased. Since the POA at such a low temperature cannot affect the interface roughness, it is confirmed that TTBS is more sensitive to the oxide "bulk" quality. Hence, it is demonstrated that TR and TTBS reflect the SiO_2/Si interface quality (including the roughness) and the oxide "bulk" quality, respectively.

4. Conclusion

A new breakdown process model, the Four Stage Model, was proposed for the ultra thin silicon dioxides, which consists of the uniform wearout, the B mode shift (partial breakdown), the local wearout and the complete breakdown. Furthermore, It is also made clear that TR (Residual Time to breakdown) and TTBS (Time To the first B mode Shift) reflect the interface quality and the "bulk" oxide quality, respectively.

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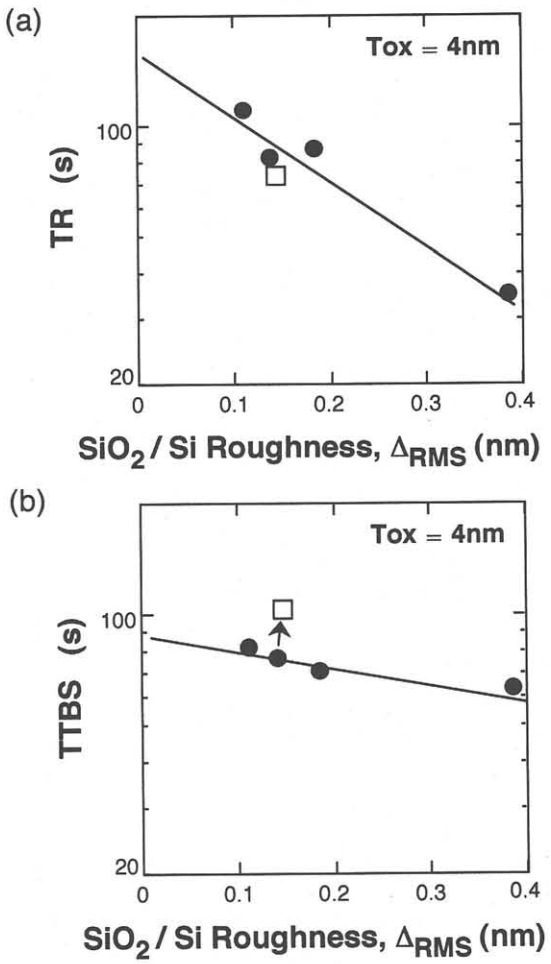

Fig. 6 (a) TR and (b) TTBS are plotted as a function of the interface roughness observed by XTEM. The sample with POA (N_2 annealing at 800°C) is indicated by □ .