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Invited

High Dielectric Constant (Ba, Sr)TiO_3 Thin Films for ULSI DRAM Application

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Investigation of high dielectric constant (Ba,Sr)TiO_3 thin films is reviewed with regard to their application to cell capacitors in high density DRAMs. The equivalent SiO_2 thickness of around 0.5nm achieved for sputtered (Ba,Sr)TiO_3 films enables a planar capacitor structure with nearly sufficient storage capacitance for 256M-bit DRAMs. As for G-bit generations, the use of a thick electrode enlarging the surface area will be a realistic approach, and hence the development of chemical vapor deposition (CVD) technology having possibility of good step coverage is desired. Through the progress in source materials and CVD systems, CVD-(Ba,Sr)TiO_3 film properties are reaching the degree of sputtered films.

1. Introduction

Despite the cell capacitor size in ULSI DRAMs is diminished with the progress of DRAM capacity, storage capacitance is needed to be maintained at around 25fF/cell. Hence, the specific capacitance per unit area is demanded to increase with increasing DRAM capacity. Figure 1 shows an estimation of required equivalent SiO_2 thickness (t_{eq}) for capacitor dielectrics in three DRAM generations with regard to various storage electrode configurations. SiO_2/Si_3N_4, which is presently used in DRAM mass-production but whose t_{eq} is limited at 5nm, seems to elongate its life up to 256M bit generation only by using a complicated scheme like hemispherical grained (HSG)-Si on cylinder structure for the enlargement of capacitor surface area. For cell capacitors in 1G bit DRAMs, as presented at the IEDM last year, the use of Ta_2O_5 having 2.5-3.5nm t_{eq} values is necessary even on the cylinder plus HSG-Si storage electrode[1,2]. It could be said that these preceding technologies have reached the ultimate stage, and hence the use of high dielectric constant materials is really desired in order to simplify the capacitor structure and processes.

In 1990, we reported on thin film preparation of (Ba,Sr)TiO_3 (BST) by sputtering, and proposed their use for the capacitors integrated in ULSI devices[3]. Compared with Pb-containing perovskite oxides such as Pb(Zr,Ti)O_3, which are alternative high dielectric constant materials studied for DRAM applications, BST has several advantages including easy control of stoichiometric composition because of not containing volatile elements like Pb, chemical stability, and paraelectric nature for appropriate Ba/Sr atomic ratio. Since the proposal described above, much effort has been directed to the preparation of high quality BST thin films by various researchers. As a result, capacitors for 64-256M bit DRAMs were demonstrated using sputtered BST thin films[4,5], and recently a capacitor for 1G bit DRAMs was presented using $SrTiO_3$ films prepared by chemical vapor deposition (CVD)[6]. In the following, preparation and properties of BST thin films are reviewed, concentrating on sputtering and CVD preparation.

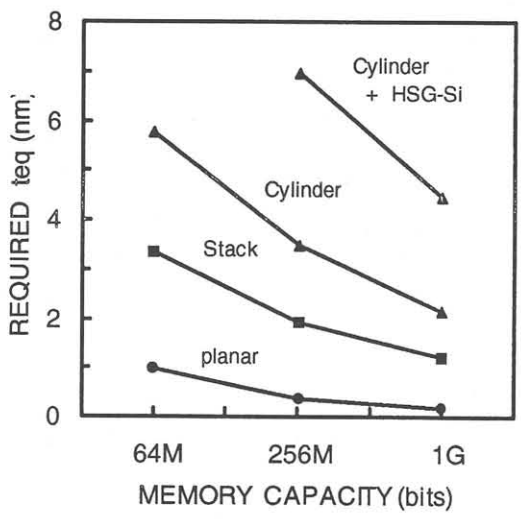

Fig.1 Required SiO_2 equivalent thickness (t_{eq}) for three generations of DRAM capacity and for various storage electrode structures. Stack means a thick electrode enabling the enlargement of capacitor surface area by using its sidewall. The height of cylinder and stack electrodes is assumed to be 0.5μm.

2. Sputtering

Sputtering deposition of BST thin films is usually performed with RF magnetron sputtering mode using oxide BST targets. Film composition almost equivalent to that for targets is obtained even at substrate temperatures as high as 600-700°C[3,7]. We studied the dependence of dielectric constant on Ba/Sr atomic ratio, and showed that the maximum dielectric constant is obtained at the ratio of 1, *i.e.* $(Ba_{0.5}Sr_{0.5})TiO_3$ composition[3]. This dependence was confirmed by Kuroiwa *et al.*[8] for RF magnetron sputtering and by Yamamichi *et al.*[9] also for ion beam sputtering (IBS) method.

Thickness dependence of dielectric constant is the most serious problem limiting the t_{eq} value of BST thin films. A dielectric constant as high as 800 is obtained at a film thickness around 500nm for the films prepared at 600-700°C[3], but a decrease in dielectric constant with decreasing thickness is usually observed. Typical data for the dependence are plotted in Fig.2 with filled squares. They were measured on films prepared by IBS method at 650°C[10], while films prepared by RF magnetron sputtering at the same temperature revealed almost the same values. As a result of the thickness dependence, the minimum t_{eq} value is limited to be 0.6nm. One possible explanation for the dependence is the existence of a low dielectric constant layer at either or both of the interfaces between a BST film and top and bottom electrodes[3]. As indicated by Dharmadhikari *et al.*[11] on a sputtered $BaTiO_3$ film, we have identified a surface layer revealing slight composition deviation from that in the main layer. We have etched out the surface layer, but have not succeeded to observe any increase in measured dielectric constant. This result implies negligible effect of the surface layer, while it would be possible that the etching induced another deterioration at the surface layer.

The data reported by Horikawa *et al.*[7] on $(Ba_{0.75}Sr_{0.25})TiO_3$ films are also plotted in Fig.2 with filled circles. The films were prepared by RF sputtering method at 660°C. The dielectric constant is a constant value 320 in the thickness range between 50 and 90nm, , and decreases only at the thickness less than 50nm. They observed a granular structure consisting of plural grains in thickness direction for the films thicker than 50nm, and attributed the thickness dependence of dielectric constant to a grain size effect, considering their another experiment showing a grain size dependence of dielectric constant. Grain size was considered to be a constant value 45nm for the films thicker than 50nm, and be equivalent to the film thickness for the films thinner than 50nm. The 0.47nm t_{eq} value was obtained for the 30nm thick film. They recently reported the value less than 0.4nm, which is the minimum value ever reported, to the best knowledge of the author. It is also noteworthy that sufficiently low leakage current was measured for the films up to 100°C

Considering the application to 1G bit DRAMs, even the above shown t_{eq} value around 0.5nm does not meet the requirement for realizing the most desirable planar capacitor structure, as seen in Fig.1. A realistic approach will be the use of a stack electrode structure, which enables the enlargement of capacitor surface area. Compared with a planar structure, it does not demand an increase in the number of process steps but does a thick electrode and results in a height difference between the cells and other areas within a chip. For this approach, CVD is considered to be desirable because of its possibility of good step coverage, and is discussed in the next section.

Yamamichi *et al.*[12] recently fabricated $(Ba_{0.5}Sr_{0.5})TiO_3$ films onto 0.5μm high RuO_2 steps by RF sputtering, and evaluated the properties of the BST films on the sidewall of RuO_2 electrodes. Thanks to a tapered etching of the RuO_2, step coverage, defined as a ratio of the thickness on the sidewall surface to that on the top surface of a step, of 50% was obtained. The dielectric constant for the films on the sidewall was evaluated to be almost the same as the value for the films with equivalent thickness on the top surface.

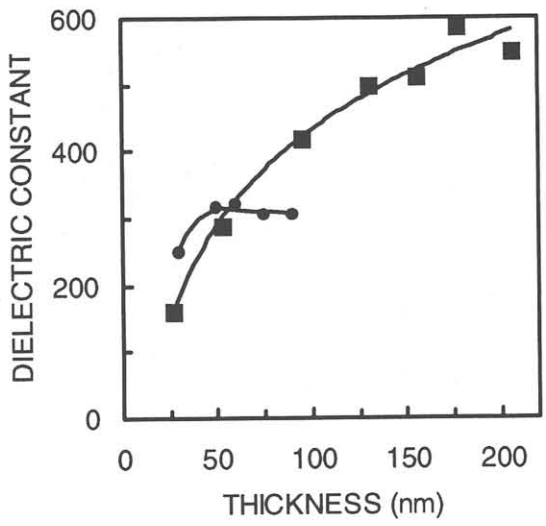

Fig.2 Thickness dependence of dielectric constant for $(Ba_{0.5}Sr_{0.5})TiO_3$ films by IBS (filled squares) and for $(Ba_{0.75}Sr_{0.25})TiO_3$ films by RF magnetron sputtering.

3. CVD

Although CVD is usually considered to have ideal features such as good step coverage, high deposition rate, and good uniformity in thickness and composition over large wafer area, difficulty of CVD preparation of BST lies in the lack of sources

for Ba and Sr having sufficient vapor pressure and stability. $Sr(DPM)_2$, or strontium bis-dipivaloylmethanate, and $Ba(DPM)_2$ are popular solid sources used in the CVD preparation of oxide superconductors. Several researchers claimed the disadvantages of the $(DPM)_2$ solid sources such as low vapor pressure and possibility of decomposition during vaporization, and hence proposed alternative source materials and/or source delivery systems. All these technologies are categorized in liquid source CVD. Kirlin *et al.*[13] developed solutions of Ba- and Sr-$(DPM)_2$ tetraglyme adducts and a novel liquid delivery system comprising a high precision liquid pump. Kawahara *et al.*[14] employed $Ba(DPM)_2$ and $Sr(DPM)_2$ dissolved in tetrahydrofuran (THF), and delivered the solutions by bubbling with N_2. Kimura *et al.*[15] proposed $Sr(DPM)_2$-$trien_2$ and $Sr(DPM)_2$-$tetraen_2$ as low melting point source materials which can be vaporized at 120-130°C and bubbled with Ar.

In our laboratory, CVD preparation of $SrTiO_3$ thin films has been investigated in both thermal mode and ECR plasma-assisted mode, utilizing $Sr(DPM)_2$ and titanium isopropoxide $Ti(i\text{-}OC_3H_7)_4$ as source materials[16,17]. Recently, stable composition control has been confirmed with regard to the ECR mode operation[18]. That is, less than 10% change in Sr/Ti atomic ratio was observed over 300 runs, where each run yielded a 100nm thick film. Crystallization into the perovskite phase was obtained at substrate temperatures higher than 450°C. The Sr/Ti ratio around the stoichiometric composition gave the maximum dielectric constant. Typical value was 150 for the films prepared at 450°C not depending on the thickness ranging 30-120nm. In the Sr-deficient region, the crystallinity degraded with decreasing Sr/Ti ratio. In the Sr-rich region, the lattice constant increased with increasing Sr/Ti ratio, which would be due to SrO layer insertion resulting in a $(SrTiO_3)_m(SrO)_n$ layered structure[16-19]. In the Sr/Ti ratio range between 0.7 and 1.2, leakage current density gradually increased with increasing Sr/Ti ratio[19]. Typical value at Sr/Ti=1 was 8×10^{-7} A/cm^2 at 1V for 40nm thick films. Step coverage was evaluated to be 40-50% on 0.3μm spaced steps with 0.5μm height[6,20]. Although the step coverage value is not as good as expected, the $SrTiO_3$ films prepared by ECR mode revealed good uniformity in thickness on the sidewall surface, while the films by thermal mode had a slight overhang at the corners of the step. This feature of the ECR mode deposition is useful for a G-bit DRAM capacitor. Because the sidewall surface area of a thick storage electrode in a G-bit DRAM is much larger than the top surface area, contribution of the top surface to the capacitance is very small, and hence the thickness uniformity on the sidewall is one of the most important factors. Preparing the $SrTiO_3$ films onto a storage electrode consisting of a RuO_2/TiN layer on poly-Si plug, possibility of fabricating a 1G bit DRAM capacitor was demonstrated[6]. It should be noted that the $SrTiO_3$ deposition at a temperature as low as 450°C enabled preventing the interface deterioration in the RuO_2/TiN/Si structure which could cause an increase in contact resistance. Specific capacitance density desired to be as high as possible for decreasing the electrode height and for affording enough process margin. In order to meet this requirement, CVD deposition of $(Ba,Sr)TiO_3$ is under study in our laboratory.

As described above, Kirlin *et al.*[13] already reported on CVD fabrication of BST films using a liquid source delivery system. They obtained a dielectric constant value of 350 for a 46nm thick film prepared at 600-740°C. Another attractive feature of the work will be a deposition rate as high as 15nm/min. Kawahara *et al.*[14] also reported on BST film fabrication employing THF dissolved liquid sources described above. They measured a dielectric constant value of 700 for a 80nm thick film having a Ba/Sr ratio of 1 and prepared at 600°C, and a value of 220 for a 48nm thick film having a Ba/Sr ratio of 0.55 and prepared at 480°C. Recently, they changed a Ti source material from titanium propoxide to a THF solution of titanium bis-isoproxy-bis-dipivaloylmethanate, $Ti(O\text{-}i\text{-}C_3H_7)_2(DPM)_2$, and improved the step coverage from 40% to 72%[21].

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