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Invited

Artificial Quantum Solids that Compute: Quantum-Mechanical Logic Gates and Neuromorphic Networks

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We will describe a novel paradigm for ultrafast, large-scale computing based on quantum-mechanical interactions between electrons confined in arrays of semiconductor or metal quantum dots. Two types of architecture will be described: (i) combinational circuits/sequential memory utilizing Boolean logic, and (ii) associative memory derived from neuromorphic implementation. Initial experimental efforts at fabricating these circuits - which we term "artificial quantum solids" - have yielded promising results.

1. QUANTUM MECHANICAL BOOLEAN LOGIC CIRCUITS

Quantum-mechanical Boolean logic circuits utilize a single electron as the basic building block. The *spin* of the electron encodes the binary bit[1)]. In a suitable array of quantum dots housing single conduction band electrons, the spin orientation of every electron becomes a bistable quantity. Logic circuits are constructed by arranging the quantum dots in different topologies on a wafer which tailors the spin-spin interactions between their guest electrons. Various topologies give rise to various interactions and thus various logic functions (AND, OR, etc.). These can be further manipulated to yield more complex circuits such as full adders and subtractors, as well as sequential memory such as flips-flops, ripple counters and read only memory (ROM)[1)]. An example is shown in Fig. 1.

In this scheme, binary signal (spin state) is communicated from one electron to the next via exchange coupling so that there is no physical wire connecting the various internal elements within a chip[2)]. Only the peripheral elements (quantum dots) on the edges of the wafer are connected to the external world and serve as input/output ports[3)]. Data is read from and and written into these dots with spin-polarized scanning tunneling microscope (SPSTM) tips[4)]. The elimination of internal physical interconnects leads to significant improvement in speed and density.

The advantage of using spin to encode binary information is manyfold. First, one does not have to *move* charge to switch a device; only the spin has to be toggled. This eliminates transit time limitations on switching speed and also problems associated with charge trapping by material defects. Second, spin cannot be flipped by electric fields resulting in excellent noise immunity. Finally, the power delay product can be 10^{-20} Joules, the switching delay can be 1 ps, the bit density can approach 10 terabits/cm^2, and most importantly, these circuits can operate at room temperature which is a distinct advantage.

2. QUANTUM NEUROMORPHIC NETWORK

In contrast to logic gates, the neuromorphic architecture exploits the collective, semi-classical charging behavior of a large number of resistively or capacitively linked semiconductor or metal quantum dots fabricated on a *non-ohmic* substrate. If the substrate has a nonlinear and *non-monotonic* current-voltage characteristic (e.g. a resonant tunneling diode or an Esaki diode), then such a system is globally stable and there are multiple equilibrium points that are necessary for non-trivial computation[5)]. We will show that such a simple system realizes the short term additive memory (STM) or the content-addressable memory (CAM) model of neural networks[6)] without requiring amplifiers or massive interconnectivity[5)]. We will also show that this simple system possesses rudimentary two-dimensional image processing capability and can solve certain NP-complete optimization problems such as the famous traveling salesman problem[5)]. An example of a quantum neuromorphic image processor that performs a "smoothing" operation with edge-enhancement is shown in Fig. 2. Finally, these circuits are also capable of room temperature operation and possess all other attractive features of quantum devices such as high speed, low power, etc.

3. CONCLUSION

In addition to describing the above schemes, we will also point out some possible pitfalls that often lead to flawed proposals in this field. We will illustrate this with some previously proposed ideas[7)] that contain one or more serious errors. Finally, we will also describe our intial efforts at experimentally fabricating artificial quantum solids using molecular-level self assembly of nanometer-scale quantum dots. This technique, unlike direct-write nanolithography, is a parallel process amenable to mass production and commercial utilization[8),9)].

4. REFERENCES

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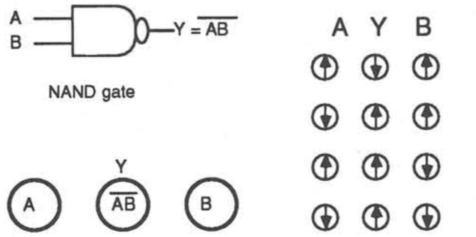
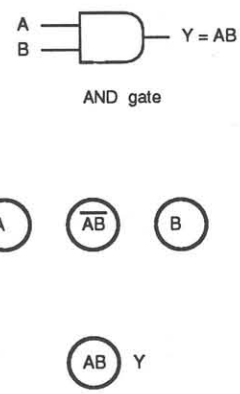


Realization of a NAND gate by a linear array of three quantum dots housing single electrons. The two peripheral dots are input portsto which binary logic variables A and B are applied by orienting the electron spins in these dots with an external source such as a SPSTM. The spin orientation of the electron in the central dot (which acts as the output port) becomes the NAND function of the spin orientations of the two peripeheral dots (inputs). The basic physics that makesthis work is the fact that nearest neighbor electrons have opposite spins because of exchange interaction.To realize this NAND functionality, an external static magnetic field must be present which slightly favors the upspin (or logic 1) state. It is easy to verify that if the direction of the static magnetic field is reversed, so that the downspin (logic 0) state is favored instead, then the same array will realize NOR functionality instead of NAND.

Possible spin configurations of the array corresponding to various combinations of binary inputs (spin orientations of the peripheral cells). This can be viewed as a truth table. It is immediately obvious that this is the truth table of a NAND gate.

Fig. 1 (a): Realization of a NAND gate



An AND gate is realized by diverting the output of the NAND through an inverter. The two vertical cells together constitute an inverter since they are nearest neighbors. Note that the output cell is further from the central cell than the two input cells so that the central cell is more strongly coupled to the inputs than to the output. **This is very important.** It emulates unidirectional "gain" between the input and output thus allowing the input to drive the output.

Possible spin configurations of the array

Fig. 1 (b): Realization of an AND gate

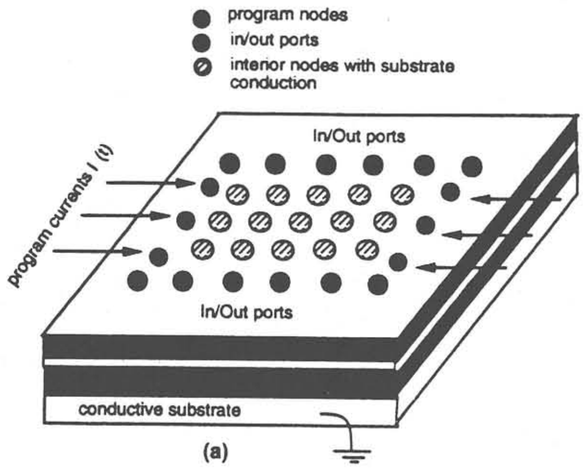


Fig. 2(a): A basic neuromorphic network consists of quantum dots arranged on a non-ohmic substrate and linked by molecular wires.

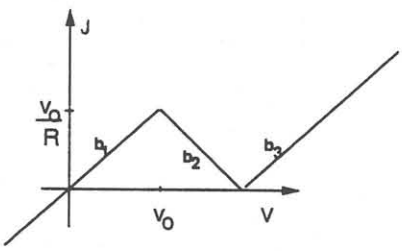


Fig. 2(b): The current voltage characteristic of the substrate has a non-monotonic non-linearity whose piecewise linear approximation is shown. The voltages on branches b_1 and b_2 are stable. This figure defines the quantities v_0 and R used in later figures.

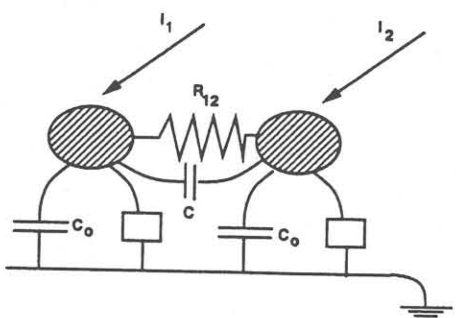


Fig. 2(c): The simplest system of two quantum dots laterally coupled by resistance R_{12} and capacitance C. The dots are also coupled to the substrate via a capacitance C_0 and a non-linear resistance characterized by the non-linearity in Fig. 2(b).

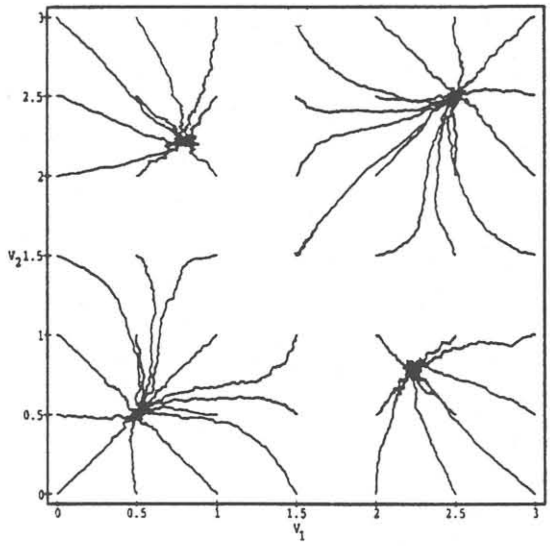


Fig. 2(d): Phase portrait for single electron charging stochastic dynamics (obtained by Monte Carlo simulation) showing the existence of four stable equilibrium points (v_1 and v_2 are the voltages on the two quantum dots in Fig. 2(c)).

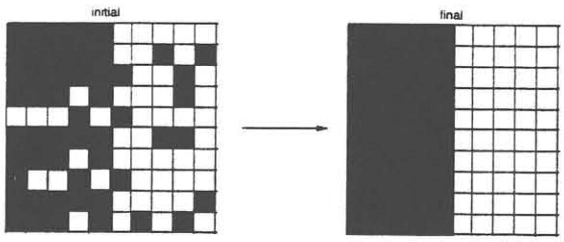


Fig. 2(e): Rudimentary image processing capability in a near-neighbor connected network of 10X10 quantum dots which are all pumped by the same current $I_0 = v_0/2R$. Current connections are made to the dots by molecular wires. Each dot is colored according to the particular branch b or b of the substrate non-linearity in Fig. 2(b) the dot potential lies on. The resistive connection between dots is uniform and has a value $R_{ij} = 6R$. The input contains domains that are either predominantly black or white and the output contains domains that are either all black or all white. This smoothing operation does edge-enhancement.