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Invited

Novel Fabrication Technique for a Si Single-Electron Transistor and Its High Temperature Operation

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A Si single electron transistor (SET) was fabricated by converting a one-dimensional Si wire on a SIMOX substrate into a small Si island with a tunneling barrier at each end by means of pattern-dependent oxidation. Since the size of the Si island became as small as around 10 nm owing to this novel technique, the total capacitance of the SET was reduced to a value of the order of 1 aF, which guaranteed the conductance oscillation of the SET even at room temperature. Furthermore, a linear relation between the designed wire length and the gate capacitance of SETs was obtained. This result indicates the high reproducibility of this fabrication technique.

1. Introduction

Considerable interest has been stimulated in the single electron transistor (SET) because it is thought to be a key element in future single electronics where many SETs would be conjunctly used as single electron memories and SET logic circuits[1,2]. In the development of single electronics, single-electron devices operable at high temperatures are strongly required. A SET operating at high temperatures must have a very small island with adjoining two very small tunnel capacitors because this structure promises to obtain the very small total capacitance of the island. Since recent advances in electron beam lithography permit a pattern size of several tens of nanometers, SETs with a very small island and very small tunnel capacitors have been successfully fabricated using a constricted pattern shape on various two-dimensional electron gases[3]. A SET fabricated by controlled lithography will be an advantage in future large sale integration of the devices. However, the island capacitance of these SETs fabricated using this technology has been limited to around 100 aF because the size of the island can not be smaller than that of the constrictions in this method. To overcome this problem, we proposed a new method to convert the one-dimensional Si wire to a very small Si island with adjoining two very small tunnel capacitors, and successfully observed the conductance oscillations even at temperatures around 300 K[4]. In this paper, we report the relationship between the Si-SET characteristics and the pattern structure of the one-dimensional Si wire.

2. Experimental

As the base material, we used a SIMOX (separation by implanted oxygen) wafer with a very smooth superficial Si/buried SiO_2 interface which was obtained by 40-h annealing at 1350°C[5]. A 30-nm-thick superficial Si layer with a 30-nm-thick top SiO_2 layer was prepared. The thickness of the buried SiO_2 layer was 400 nm. In order to fabricate the one-dimensional Si wire, we used electron beam (EB) nanolithography combined with an image reversal process using ECR (electron-cyclotron-resonance) plasma oxidation[6]. The fabrication process is as follows. Just after the deposition of a 40-nm-thick amorphous Si (a-Si) layer on the top SiO_2 layer, a 50-nm-thick positive resist was coated on the a-Si layer, and then the resist pattern shown in Fig. 1 was formed by EB lithography. Here, the resist on the one-dimensional wire and two-dimensional source and drain regions was removed and the surface of the a-Si on the area appeared since these areas were exposed to the EB. Then, the a-Si surface was oxidized by an ECR-O_2 plasma stream, where the lateral shrinkage of the resist pattern due to O_2-plasma etching was very small because of the highly directional nature of the ECR plasma stream. Next, the resist was removed with acetone to avoid oxidizing the a-Si surface under the resist. The a-Si layer was etched by ECR Cl_2-based plasma using very thin plasma-oxidized SiO_2 as a mask. Then, the 30-nm-thick SiO_2 layer and the superficial Si layer were etched by RIE and ECR Cl_2-based plasma using a-Si and SiO_2 as a mask, respectively. The one-dimensional Si wire with the two-dimensional Si layers for the source and drain regions was formed, on which the SiO_2 layer remained. However, the a-Si layer was completely removed by the final ECR etching.

The width of the wires was 20 nm while the length *Ld* varied in the range of 50-200 nm. The width of the two-dimensional regions which were connected to each end of the wire was 400 nm. After the pattern was formed, the wafer was oxidized in a dry oxygen ambient at 1000°C, which not only reduced the width and height of the wire, but constricted the wire at its ends by means of pattern dependent oxidation[4]. In the oxidation process, oxygen atoms penetrate into the buried oxide layer through the slits opening on the Si layer, and oxidize the superficial Si layer from the back side. This makes the Si layer thinner along the pattern edge. Figure 2 shows the one-dimensional wire and two-dimensional regions after thermal oxidation. The hatched regions indicate the area oxidized more from the backside. On the other hand, in the center region of the Si wire, oxidation is suppressed by the stress accumulated during oxidation. Consequently, constricted regions are

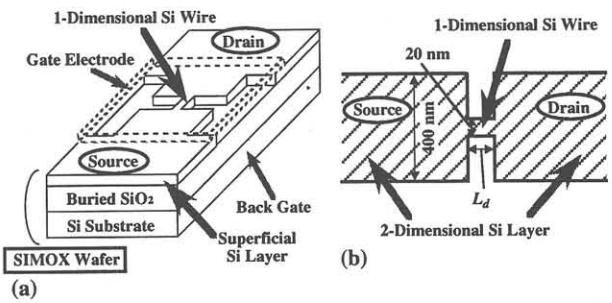

Fig. 1. Schematic diagram of a Si-SET (a) and EB pattern (b). The width of the wires is 20 nm long while the length *Ld* is varied in the range 50-200 nm. The width of the symmetric two-dimensional Si-MOS structures which are connected to each end of the wire was 400 nm. Here, the gate oxide is not shown for simplicity.

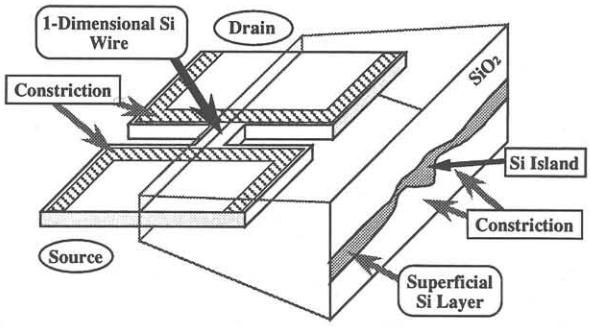

Fig. 2. (a) Cross-sectional view of the SET and (b) equivalent circuit. The Si island is surrounded by the gate electrode, substrate Si under the SiO_2 layer, and source and drain regions

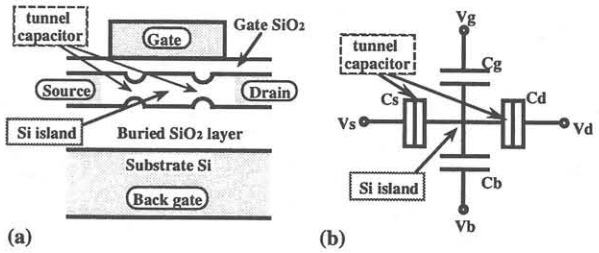

Fig. 3. Schematic diagram of the one-dimensional wire and two-dimensional regions and its cross section after thermal oxidation.

formed at the ends of the wire as shown in the cross-sectional view in Fig. 2. This process converts a narrow Si wire into a very small Si island because both constricted regions produce potential barriers by means of the quantum size effect[4]. Here, the width of the two-dimensional regions connected to the wire is very important in oxidizing the ends of the wire effectively because the oxygen diffusion from both sides of the two-dimensional regions promotes the oxidation from the back side at the ends. It seems that the width of 400 nm is a suitable size in the case of the oxidation condition used here. Finally, the SET fabrication was completed after the phosphorous-doped poly-Si gate electrode was formed over the wire as shown in Fig. 1, followed by the phosphorous ion implantation for the source and drain regions, and aluminum electrode formation. Figure 3 shows the schematic cross section of the SET and equivalent circuit. In this structure, the island was completely covered by the four electrode (gate, source, drain, and backgate electrodes). Here, the backgate capacitance can be disregard because it is as small as 1/30-1/10 of the gate capacitance[4].

3. Results and Discussion

The source-drain conductance was derived from *I-V* characteristics measured with an HP 4156A precision semiconductor parameter analyzer. The conductance as a function of the gate voltage is shown in Fig. 4 for SETs with a wire length Ld of 70 nm or 100 nm. Here, the drain voltage was 1 mV, and the source and backgate (substrate) voltages were fixed at 0 V, and the device temperature was 30 K. The conductance characteristics at various temperatures for SETs with a wire length Ld of 50 nm are shown in Fig. 5. Clear conductance oscillations are observed even at high temperatures of 30 K and above. These oscillations are due to the Coulomb blockade by tunneling barriers with a very small capacitance fabricated by the procedure described above.

The gate capacitance Cg is estimated from the conductance oscillation period ΔVg in the gate voltage according to $Cg=e/\Delta Vg$. Despite the same designed wire length Ld, the oscillation period between the devices is different. For example, the gate capacitance of SETs shown in Fig. 4 and 5 is calculated to be about 0.05 aF and 0.5 aF for Ld=50 nm (Fig. 5 (a), (b)), 0.6 aF and 1.5 aF for Ld=70 nm (Fig. 2 (a), (b)), and 1.5 aF and 1.7 aF for Ld=100 nm (Fig. 2 (c), (d)). These differences might be caused by the fluctuation of the length, width and height of the wire. We estimate the final width and height of the Si island to be about 5-10 nm. The standard deviation σ of the superficial Si thickness is about 0.4 nm which was obtained from the surface topography of the top surface of the superficial Si layer and the buried oxide layer measured by atomic force microscopy (AFM). The σ of the pattern width defined by EB lithography is about 2-3 nm which was also obtained from the AFM measurements. Since the capacitance of the Si island must be proportional to the size of the wire, the fluctuation of the oscillation period is estimated to be about ±50%.

In spite of this fluctuation, a clear feature observed is that a shorter wire length yields a smaller gate capacitance, or a longer oscillation period. Figure 6 shows the gate capacitance Cg as a function of the designed wire length Ld.

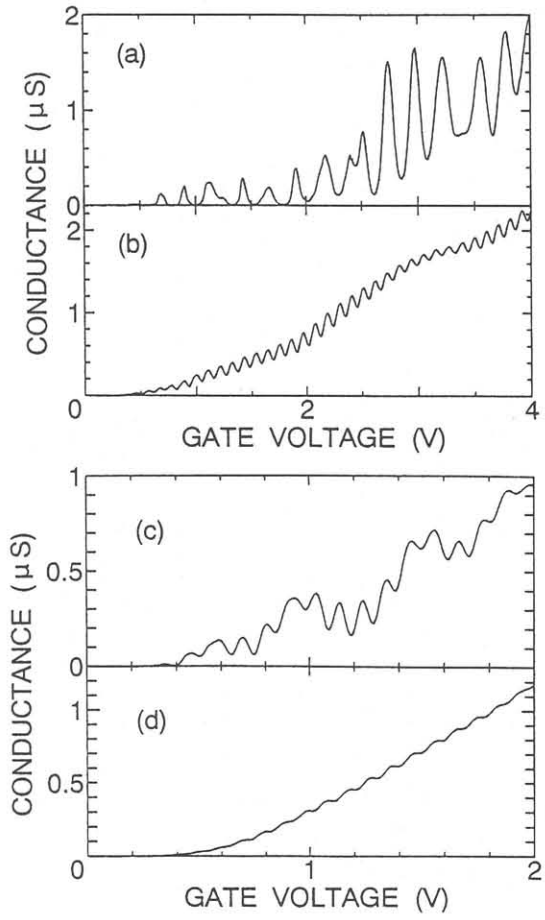

Fig. 4. Conductance oscillations as a function of the gate voltage Vg measured at 30 K. (a), (b) Ld=70 nm and (c), (d) Ld=100 nm.

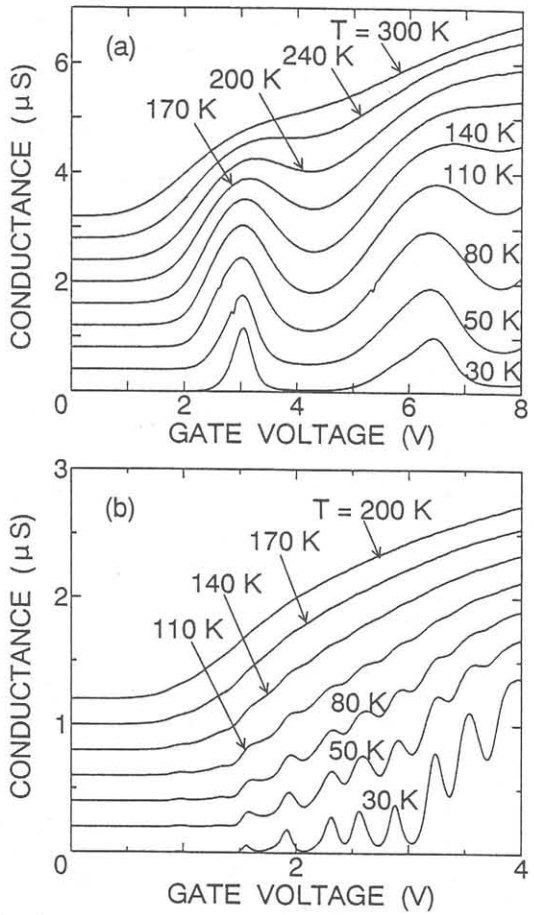

Fig. 5. Conductance oscillations of SETs (a) and (b) with Ld=50 nm at various temperatures. The curves are offset vertically.

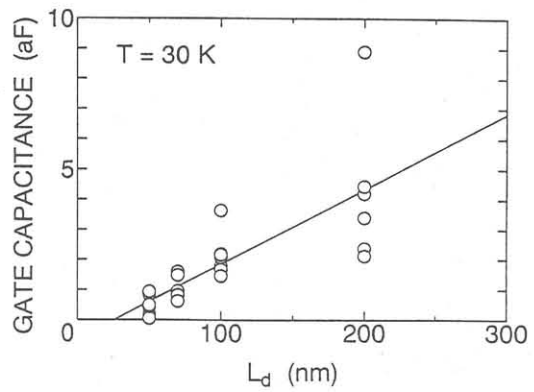

Fig. 6. Relation between the gate capacitance Cg and the designed wire length Ld. The designed wire width is 20 nm, and the width of the two-dimensional regions which are connected to each end of the wire is 400 nm.

In these SETs, clear conductance oscillations are observed. An almost linear relation between Cg and Ld is seen, which can be expressed by

$$Cg = A\ Leff, \qquad (1)$$

$$Leff = (Ld - Loff), \qquad (2)$$

where $Leff$ is the effective length of the island after thermal oxidation and A is the capacitance per unit length. From Fig. 6, an $Loff$ of 26 nm and an A of 0.025 aF/nm are obtained. The value of $Loff/2$ means that each tunnel barrier edge intrudes into the wire by about 13 nm. Furthermore, the very small value of A indicates that the very narrow wires were successfully fabricated.

The conductance oscillations remain even at 300 K for the SET in Fig. 5 (a), though it almost disappears at around 200 K for the SET in Fig. 5 (b). From these data, the total capacitance of these SETs in Fig. 5 (a) and (b) are estimated to be about 1.5 aF and 3 aF, respectively. Here, we assumed that the oscillation disappears at the temperature T where $4kT$ is equal to the Coulomb gap ($e/Ctotal$) of the SET, taking thermal smearing of the Fermi distribution function into account[7]. The total capacitance of about 3-5 aF is the average value for the SETs with an Ld of 50 nm. If we assume the island to be a sphere with a radius of r, the capacitance is roughly given by

$$Ctotal = 4\pi\varepsilon\varepsilon_0 r\,. \qquad (3)$$

Here, ε=3.9 assuming SiO_2 is the dielectric material around the Si island. According to this equation, the total capacitance of 4 aF corresponds to the diameter of the sphere of about 20 nm. In this estimation, we have chosen a SET with an Ld of 50 nm because the shape of the island seems most like a sphere in our SETs, and the capacitance evaluation of a longer island is very difficult due to its complicated electrode configuration. In spite of this rough estimation, this sphere size agrees well with the $Leff$ of 24 nm.

4. Conclusion

SETs with very small tunnel capacitors can be fabricated by controlling the structure of a very thin wire-patterned Si layer using pattern-dependent oxidation. Using this novel technique, the total capacitance of a SET can be reduced to a value of the order of 1 aF since the size of the Si island is as small as around 10 nm. Furthermore, the reproducibility of this technique is confirmed from the linear relation between the designed wire length and gate capacitance. This is achieved due to the controllability of the fabrication process based on the thermal oxidation of Si.

Acknowledgment

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