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Novel Schottky In-Plane Gate Single-Electron Transistors Using GaAs/AlGaAs System Operating up to 10K

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The novel Schottky in-plane-gate (IPG) single-electron transistors (SETs) were successfully fabricated by applying an *in-situ* electrochemical process to AlGaAs/GaAs two-dimensional electron gas (2DEG) wafers. The fabricated devices showed clear Coulomb blockade oscillation and Coulomb staircase characteristics. Coulomb blockade oscillation was observed up to 10K. This temperature is much higher than that of the previous split-gate devices having the sample lithography dimensions.

1. Introduction

For realization of integrated Single Electronics operating at room temperature, single-electron devices (SED) should not only work at room temperature, but should be designable and manufacturable with acceptable uniformity and reproducibility. Recently, high-temperature operation of SEDs have been reported, but they seem to rely on spontaneous dot formation in poly-crystalline grains, on dot formation by spontaneous oxidation or on potential variation caused by impurity doping. On the other hand, GaAs-based well-defined transistor structures using split gates operate only in mK range.

The purpose of this paper is to demonstrate that the novel Schottky in-plane-gate (IPG) single-electron transistor (SET) produced by applying our *in-situ* electrochemical process to AlGaAs/GaAs two-dimensional electron gas (2DEG) wafers operates at much higher temperatures than the split-gate devices and may fill the above mentioned technology gap by further size reduction.

IPG quantum structures[1,2] based on lateral field effects are attractive since they can produce strong lateral fields that confine electrons within a quantum wire or dot, and realize large separations of subband energies. Such strong confinement is essential in order to construct quantum devices which operate at high temperatures. However, previous IPG SETs[3] utilized semiconductor-insulator-semiconductor (SIS) IPG realized by traps produced by high-energy focused ion beam (FIB). In the present novel device, Schottky IPG gates were formed by the low-energy *in-situ* electrochemical process which have recently produced oxide-free, defect-free nearly ideal thermionic Schottky contacts to GaAs[4,5], to InP[6] and to 2DEG in AlGaAs/GaAs quantum wells (QWs)[7].

2. Fabrication process

The structure of the novel Schottky IPG SET is schematically shown in **Fig. 1(a)**. The $Al_{0.3}Ga_{0.7}As$/GaAs double-hetero structure QW wafers with a Si delta-doped layer were grown by the standard molecular beam epitaxy (MBE) technique at 580°C. Hall mobility μ_{Hall} and sheet carrier density n_s of the structure were typically in the range of $5\sim8\times10^4$ $cm^2 \cdot V^{-1} \cdot s^{-1}$ and $5\times10^{11}\sim1\times10^{12}$ cm^{-2} at 77K, respectively. On the top of the epitaxialy grown layer, SiO_2 was deposited by photo-chemical vapor deposition and used as a passivation film. Then, a heterostructure wire was formed by electron beam (EB) lithography and wet chemical etching. The beam energy was 25 keV and ZEP-520 resist (Nippon ZEON) was used as the EB resist.

The window pattern for gates, shown in **Fig. 1(b)**, was also directly written by EB lithography followed by the formation of Pt Schottky IPG electrodes by the *in-situ* electrochemical process which consists of anodic etching to remove oxide and subsequent cathodic deposition of Pt. Owing to the presence of the top SiO_2 layer, Pt was not deposited on the top of channel, but only on the sides of channel, although the plating pattern was open on the top. Thus, the novel process enables one to form IPGs without precise alignment of the mask pattern to the edge of the channel.

Figure 2 shows the SEM image of the fabricated IPG SET together with its schematic representation. Approximate sizes from SEM observation are also given. The width of finger

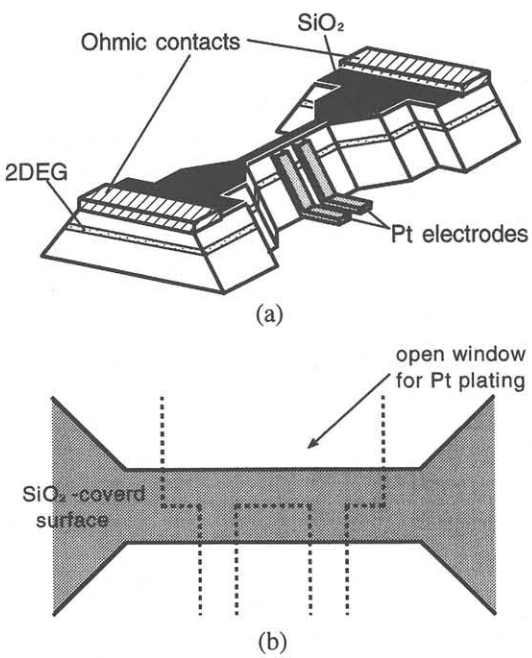
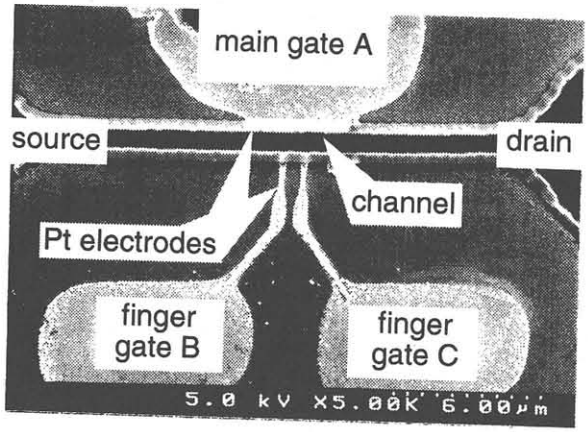


Fig. 1 (a) The scheme of single-electron transistor with Schottky IPGs. (b) Window pattern for Pt plating.



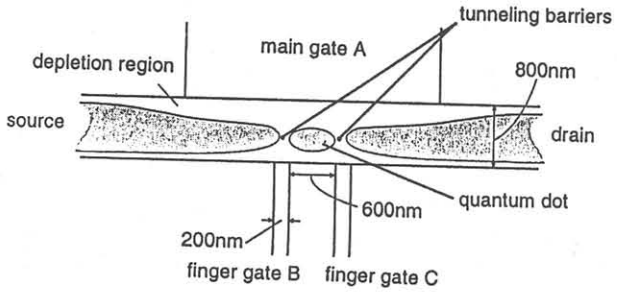


Fig. 2 SEM image and its schematic illustration of the fabricated IPG SET.

gates (B and C) as narrow as 200nm were successfully realized by Pt plating. Quantum dot and tunneling barriers are expected to be formed in the channel by applying suitable negative voltages to IPGs.

3. Device characteristics

The I-V measurements were performed on the fabricated IPG SETs by using the HP4156A semiconductor parameter analyzer. First, the drain I-V characteristics were measured, setting a voltage, V_{GA}, of main gate A as a parameter. The IPG SET devices exhibited reasonably good field-effect-transistor (FET) operation at 4.3K, as shown in **Fig. 3**. It has been shown [8,9] that the gate control of the drain current is achieved by the depletion behavior of the direct Schottky/2DEG contact.

Then, the drain current was measured in detail as a function of V_{GA} near pinch-off. The finger gates voltage and drain-source voltage were set to be constant. The IPG SET showed clear Coulomb blockade oscillations below 2K as shown in the examples shown in **Fig. 4(a)** and **(b)**. Such Coulomb blockade oscillations with the same period were reproducible even if the devices were warmed to room temperature and cooled again. For the single electron tunneling to take place, the conductance should be much smaller than the quantized conductance, $G_Q=e^2/h$. The measured amplitudes of the Coulomb oscillations were usually only a few percent of G_Q or below, being consistent with this requirement. The shape and

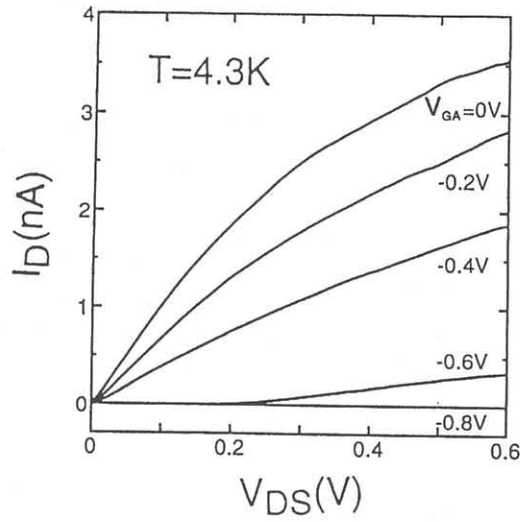
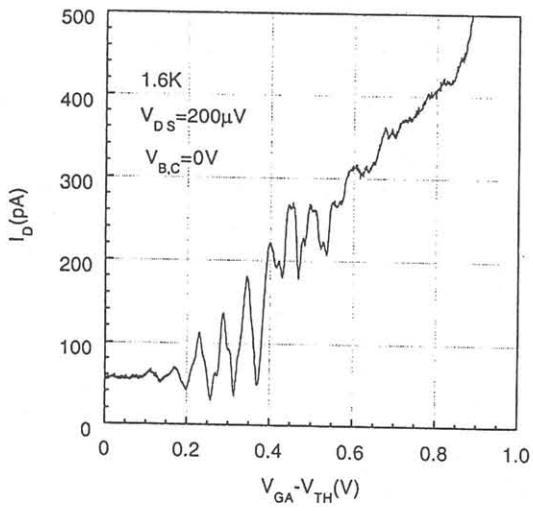
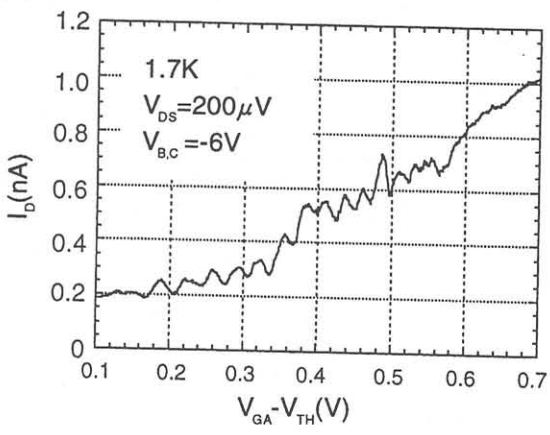


Fig 3 FET characteristic at 4.3K



(a)



(b)

Fig. 4 Coulomb blockade oscillation at low temperature. The bias conditions are different in (a) and (b).

period of Coulomb blockade oscillation could be varied by changing the bias condition, as seen in **Fig. 4(a)** and **(b)**. This indicates that the dot size and the shape and height of the tunneling barrier can be easily controlled by changing the bias conditions to the Schottky IPGs.

The fabricated Schottky IPG SETs also showed clear Coulomb staircase characteristics with many steps as compared with the split gate device, as shown in **Fig. 5**. This is due to the fact that high and thin tunneling barriers are maintained against drain bias in the present device owing to the strong lateral confinement of the IPG structure. On the other hand, tunneling barriers are easily collapsed with the increase of source- to-drain bias in the split-gate devices due to low and thick barriers.

According to theory, each voltage period shown in Fig. 4 corresponds to a charge of one electron in the dot. From the period, $\Delta V_G \approx 50$mV, a capacitance between the dot and the gate is calculated to be $C_G \approx 3$aF. The total capacitance of the dot is calculated to be $C_\Sigma \approx 500$aF from the drain voltage interval of $\Delta V_\Sigma \approx 0.3$mV in Fig. 5. The values of C_G and C_Σ are in reasonably agreement with the result of computer simulation solving the Poisson's equation for the present structure and sizes. The total capacitance value is also within a factor of 2 of the self capacitance C_0 estimated from the device size. The value of the temperature, T_0, corresponding to the charging energy is calculated to be 1.9K.

The advantage of the present Schottky IPG device based on depletion is that the effective dot size can be controlled by the bias condition. By further adjusting the bias condition, the operation temperature could be made higher at the sacrifice of reduced current as shown in **Fig. 6**. Reduction of current is due to the increased width of tunneling barriers. Under this bias condition, Coulomb oscillation was observed up to 10K in spite of a rather large lithography dimension of 600nm between two finger gates.

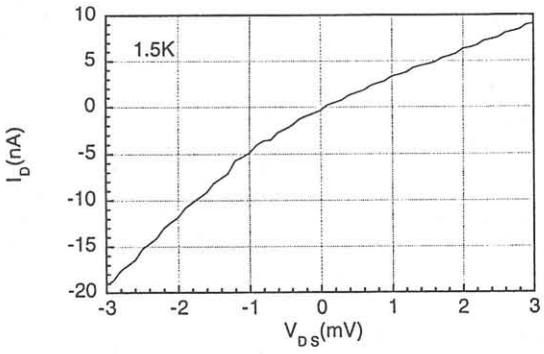


Fig. 5 Coulomb staircase at 1.5K.

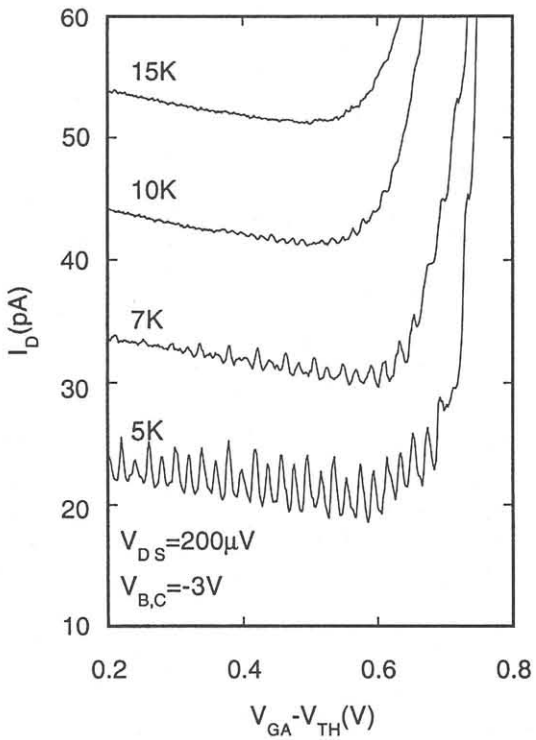


Fig. 6 Temperature dependence of Coulomb oscillation.

4. Conclusion

The novel single-electron transistor (SET) with Schottky IPGs was successfully fabricated by EB lithography and the *in-situ* electrochemical process. This device showed clear Coulomb blockade oscillations and Coulomb staircase characteristics at low temperatures. Coulomb blockade oscillation was observed up to 10K by adjusting the IPG bias condition, i.e., controlling the effective dot size. The present Schottky IPG technology seems to be very promising for the fabrication of a new class of quantum devices. Computer simulations indicates that use of EB-feasible smaller device dimensions may eventually lead to room-temperature operation.

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