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Sub-0.2um Silicon-On-Insulator (SOI) CMOS: Opportunities and Challenges

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Silicon-on-Insulator (SOI) technology has long been recognized as a potential challenger to bulk silicon as the substrate choice for the 0.25 μm lithography generation and below. This paper reviews several of the critical intrinsic device issues surrounding SOI technology, the recent progress in terms of device physics understanding in the deep-submicrometer regime, and the potential challenges that still remain.

1. Introduction

As feature sizes are scaled to smaller and smaller dimensions, considerable challenges arise in the area of device design and integration. Recent literature has suggested that silicon-on-insulator (SOI) technology can provide additional leverage in terms of performance and scalability for high-performance and low-power applications[1,2]. This paper reviews some of the critical intrinsic device issues surrounding the integration of SOI technology into mainstream applications including the deep-submicrometer device design focusing on the tradeoffs between full and partial-depletion, the self-heating effect, and hot-carrier reliability issues.

2. Deep-Submicrometer Device Design

It has long been reported that SOI offers unique options for scaling devices into the sub-0.25 μm regime. The primary issue as in bulk technologies is the control of short-channel effects. In SOI, the primary device design options are the choice between full and partial-depletion; tradeoffs between channel doping concentration, silicon film thickness, gate oxide thickness, and buried oxide thickness; and the option of using novel gate materials to engineer the metal-to-semiconductor work function.

(a) Fully-depleted device design

It was previously suggested that fully-depleted devices offer the advantages of improved short-channel effects and thus improved scalability into the deep-submicrometer regime[3], as well as improved performance due to better coupling between the gate and surface potential which results in ideal *long-channel* subthreshold slope[4] and higher drain saturation current[5]. However, although these advantages were realized in the 0.5 μm regime, as channel lengths are scaled, these relationships are modified.

Figure 1 shows the threshold voltage rolloff due to the short-channel effect vs. SOI silicon film thickness for different channel doping concentrations compared to a bulk technology with a junction depth of 80 nm. As shown, the fully-depleted device technology only exhibits improved short-channel effects over the bulk device when the silicon film thickness is significantly thinner than the bulk junction depth[6]. Comparing a fully-depleted SOI device with the same junction depth/silicon film thickness as a bulk device, the SOI device exhibits *worse* short-channel effects. This is physically due to a two-dimensional charge sharing through the SOI buried oxide that is not present in the bulk device. For 0.1 μm effective channel length, silicon film thicknesses on the order of 25-35 nm are required to achieve acceptable threshold voltage and short-channel effects for fully-depleted devices (Fig. 2). Likewise the near-ideal subthreshold slope can only be achieved when charge-sharing is completely suppressed so for short-channel devices, the subthreshold slope is typically close to the bulk value[7]. Given these effects, the traditional "advantages" of fully-depleted SOI are not realized at the deep-submicrometer dimensions.

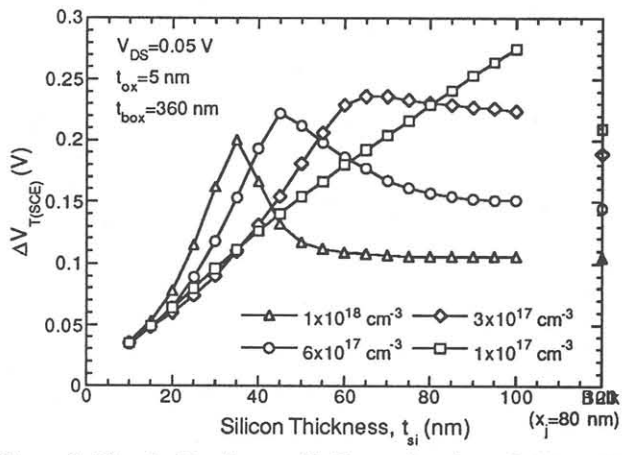

Figure 1. Threshold voltage rolloff as a function of silicon film thickness, $\Delta V_{T(SCE)} = V_T(L_{eff}=1\ \mu m) - V_T(L_{eff}=0.1\ \mu m)$[6].

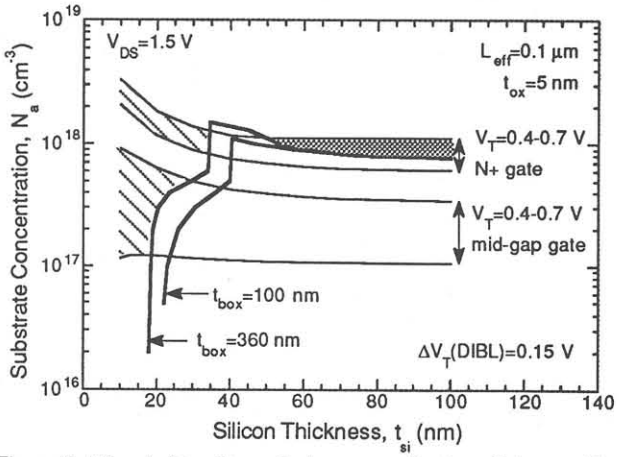

Figure 2. Threshold voltage design curve for L_{eff}=0.1 μm. V_T at V_{DS}=0.05 V defined in lighter lines, and "acceptable" drain-induced barrier lowering (ΔV_T(DIBL)<0.15 V) region defined in heavy lines. Dashed region correspond to intersection of acceptable nominal V_T and DIBL for fully-depleted devices, shaded region corresponds to acceptable design region for partially-depleted devices[6].

The requirements of such thin silicon films in fully-depleted SOI device design place some constraint on the manufacturability of the technology. The silicon thickness uniformity has been raised as a concern for fully-depleted devices because both the threshold voltage as well as the short-channel effects are critically dependent on the film thickness value. Recent advances in the materials area have demonstrated impressive silicon film thickness uniformity where 3 sigma range of less than 2.5 nm is targeted on a 200 mm wafer[8]. In addition, the device sensitivity to the silicon film thickness can be minimized by appropriate channel doping design using a 'constant dose' methodology[9]. However, the ability to control the silicon thickness in the 30 nm range on a reproducible basis and the quality of the silicon film so close to the buried oxide interface is still of some concern.

Another key issue for the use of thin silicon films in high-performance applications is the formation of salicide (self-aligned silicide). Figure 3 shows the dependence of the series resistance vs. silicide thickness for a SOI film thickness of 50 nm. To maintain a low series resistance, the silicide thickness should be chosen such that the thickest possible silicide is used to achieve the lowest sheet resistance without fully consuming the silicon film. This has been demonstrated in fully-depleted devices with 60 nm silicon film thickness by using a Ti/Co laminate process to achieve silicide thicknesses of 20-30 nm[10]. However, for silicon film thicknesses on the order of 25-35 nm (silicide thickness of 10-15 nm), there are challenging materials issues involved in forming ultra-thin silicides reproducibly. In addition, direct silicidation of the source/drain and gate simultaneously will result in a technology integration issue because the gate resistance will be limited by the thickness of the source/drain silicide. As an alternative, selective-epi or selective tungsten techniques have been demonstrated on thin SOI films[11,12], however these techniques are not necessarily available or straightforward as process modules in the generic 0.25 μm CMOS fabrication line.

Given these formidable technology integration issues, although fully-depleted devices are more "ideal" in terms of the simplicity of the device structure, it is unlikely that the technology will be mature enough for large-scale production in the near future.

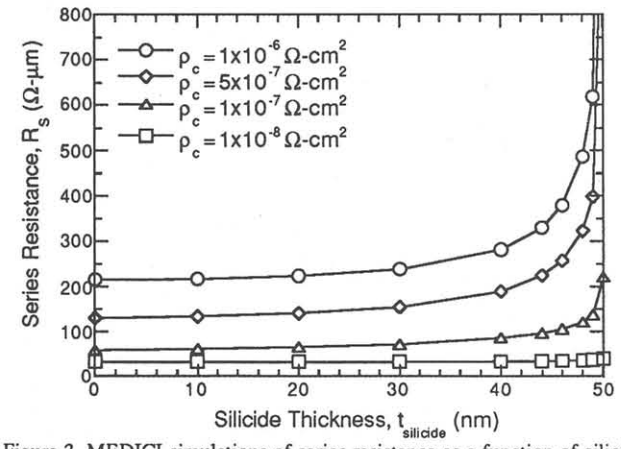

Figure 3. MEDICI simulations of series resistance as a function of silicide thickness for various contact resistivities(t_{Si}=50 nm)[10].

(b) Partially-depleted device design

In partially-depleted devices, the primary advantages of SOI are the reduction of the junction capacitance and the elimination of the body effect. However, the device design is not driven by silicon film thickness scaling. The design of the partially-depleted device is inherently very similar to a conventional bulk device. Typically the SOI film thickness is above 100 nm, and the control of threshold voltage and short-channel effects is accomplished by channel and source/drain engineering. Partially-depleted SOI devices with effective channel lengths of 0.1 μm and below have been demonstrated using super-steep retrograde channel doping and a halo/extension technology to control short-channel effects[2].

The main question surrounding the use of partially-depleted devices is the severity of the floating body effects. Floating body effects reduce the breakdown voltage[13], cause a "kink" in the DC drain current characteristics[14], and potentially reduce circuit stability due to transient effects[15,16]. Various methods for improving the breakdown voltage including bandgap engineering[17], lifetime killers[18], and special structures have been proposed[19]. But, the breakdown voltage from most reports with effective channel lengths in the 0.1-0.2 μm regime is still typically around 3 V or lower[2,17]. This makes SOI technology most useful for supply voltages of 2 V or less to allow acceptable margins for supply voltage tolerances and burn-in screening.

The key question surrounding the use of partially-depleted devices is the transient behavior of the floating-body induced effects and the severity of any circuit instabilities that may occur. Drain current overshoot in partially-depleted devices occurs as the gate voltage is pulsed because of the finite time required to redistribute holes in the body (driven by the hole recombination rate)[15,20]. Modeling has also shown that the "kink" effect arises from impact-ionization generated holes in the body that charge the floating-base of the bipolar[21]. The time constant of both of these processes determine the current drive of the device under circuit operating conditions.

Recently, measurements and modeling have shown that the impact-ionization driven charging transient is on the order of microseconds and is dependent on the device bias conditions[22,23]. This indicates that the kink-related phenomena may not be present under typical digital operating conditions. This is also supported by SOISPICE simulations and measurements of the current dissipation in inverter chains as a function of frequency[16,24]. However, the dependence of these transient effects on the period and duty cycle of typical digital circuits is still unknown. Accurate device and circuit simulations and measurements under transient conditions are required to fully evaluate the magnitude and impact of these effects.

3. Self-Heating Effects

DC self-heating has also been reported as a potential concern for SOI because of the low thermal conductivity of the underlying silicon dioxide layer (two orders of magnitude less than that of silicon). DC channel temperatures have been directly measured with special test structures and are a sensitive function of device structural parameters such as silicon film thickness and buried oxide thickness[25]. However, although self-heating reduces the DC current drive as evidenced by the negative differential conductance typical of SOI device I-V curves, the thermal time constants (on the order of several hundred ns) are also long compared to typical

electrical operating periods as shown in Fig. 4. Calculations indicate that the temperature rise under AC operating conditions should only be minimally higher than bulk substrate temperatures[25]. This is further aided by the fact that the current SOI trends are towards low-voltage, thicker silicon films (partially-depleted devices), and thinner buried oxides (to reduce material cost) all of which reduce self-heating.

The key impact of self-heating on the integration of SOI is the need to extract AC model parameters for use in circuit simulation. This can be done using both pulse measurement techniques[26] as well as through device modeling given an experimentally extracted thermal resistance[27]. Coupled with the transient floating body issue in the partially-depleted device, this highlights the need for accurate device and circuit modeling under AC conditions to make SOI a viable technology.

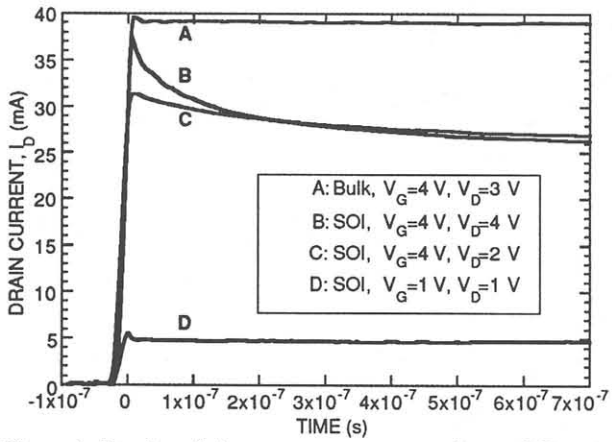

Figure 4. Transient drain current measurements for an SOI device at various power dissipations and a bulk device for comparison (L_{eff}=0.35 μm, W=50 μm, t_{si}=60 nm, t_{ox}=9 nm)[27].

4. Hot-Carrier Reliability

Finally, in the area of hot-carrier effects, there have been numerous studies examining the SOI device reliability and lifetime. This issue is complicated in SOI because substrate current, a convenient monitor of electric field in bulk devices, can not be measured accurately in SOI devices. In addition, SOI devices have both a front and back-interface which could influence device degradation.

Many unique results have been shown in terms of the hot-carrier effects on SOI, for instance the SOI electric field can be modulated by the back-gate bias which influences the gate current collected and the device degradation[28]; the electric field and degradation is strongly influenced by the non-local effect and appears to decrease with decreasing silicon film thickness in fully-depleted devices[29,30]; and degradation of the buried oxide can be significant under certain bias conditions[31].

However, the key conclusions that can be drawn based on the current literature are that: (1) under typical circuit operating conditions, (zero back-gate bias, drain voltage less than breakdown), the mechanisms of device degradation are similar to bulk MOSFETs, i.e. interface-state generation dominates NMOSFET degradation and electron trapping in PMOSFETs[32,33] (2) back-interface degradation does not appear to be a strong factor in NMOSFETs for fully or partially-depleted devices[28], although it does contribute to the degradation in fully-depleted PMOSFETs due to interface coupling[32,33] and (3) it is important that devices not be stressed in the breakdown condition when assessing SOI reliability because SOI devices have a naturally lower breakdown voltage due to the floating-body effects. Given the transient effects of the floating-body under circuit operating conditions, it is likely that the full evaluation of SOI hot-carrier reliability must also include circuit-level AC hot-carrier stress as is being pursued in bulk devices.

6. Conclusions

In conclusion, much progress has been made recently into understanding the SOI device physics at the deep-submicrometer dimensions. It appears that partially-depleted SOI offers the most scalable SOI device design although the transient floating-body effects must be assessed in a circuit environment. For SOI devices and circuits, the key challenge is to develop the modeling infrastructure on a comparable level to the existing bulk tools to understand device and circuit operation under AC conditions.

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