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# Active Matrix Liquid Crystal Displays(AMLCD's) and Active Matrix Electroluminescent (AMEL) Displays Using Silicon-On-Insulator(SOI) Technology

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At the present time Silicon on Insulator (SOI) material is being used to fabricate flat panel displays for use in projection and head mounted displays. It is expected that these displays will be applied to High Definition TV and virtual reality systems. SOI Technology brings several advantages to the manufacture of flat panel displays such as high functional density, high performance, and high voltage. This paper will discuss SOI flat panel technology and its applications.

## 1. Introduction

Flat panel displays have generated great interest within the Integrated Circuit (IC) community especially for applications in projection displays. This is a result of the use of IC processing lines, which were once thought to be out of date, to now make small projection displays. IC fabrication facilities can be converted to be compatible with quartz substrates with are used to manufacture small LCD's using polycrystalline silicon as the "active" material. This approach was first used by Seiko-Epson for the manufacture of their LCD watch and later by them to make small direct view TV's. Amorphous silicon is presently being used as the active material in the fabrication of direct view displays as well as some projection displays. Amorphous silicon technology, however, does not lend itself to Integrated Circuit type processing since it includes plasma deposited amorphous silicon, refractory metals, and no diffusion processes.

Recently single crystal silicon-on-insulator material has been used for the fabrication of flat panel displays.[1-2] This material has been used for a number of years for the fabrication of high speed and radiation tolerant IC's. It's use in LCD's was first demonstrated by a combined effort between Kopin Corp., The Sarnoff Center, and Standish Industries. It's use in electroluminescent (EL) displays resulted from a combined effort between Kopin, Sarnoff, Planar America, and Allied-Signal. In this paper we will discuss the work that has been done in both LCD's and AMEL displays using single crystal silicon material.

## 2. Active Matrix Electroluminescent Displays

Electroluminescent (EL) flat-panel displays offer many advantages including, self-emissivity, high-brightness, light-weight, ruggedness, and low-power consumption. Because of the high drive-voltage (typically>200V) and perceived incompatibilities between EL and silicon processing, EL displays are most commonly driven using passive techniques. These schemes have the disadvantages of 1)requiring a large number of interconnects which limit pixel density and potentially impact reliability, 2)higher power dissipation in the panel, and 3) limited brightness. Active-matrix techniques using a-Si:H[3], Poly Si[4], and CdSe[5] TFTs have proven feasible. Due to low carrier-mobility and/or threshold instabilities inherent in devices made from these materials, however, AMEL arrays with on-board peripheral circuitry (scanners) have not proved feasible. The purpose of the present work is to alleviate these problems by, for the first time, demonstrating a fully scanned, high-density, active-matrix, electroluminescent display using single-crystal silicon-on-insulator high-voltage IC technology.

## 3. Active-Matrix AMEL Pixel Circuit

Fig. 1 is a diagram of the AMEL pixel circuit. N1 is the low-voltage access transistor and can be either NMOS or PMOS. N2, is the n-channel, high-voltage driver transistor, fabricated using the well-known double-diffused MOS (NDMOS) approach.

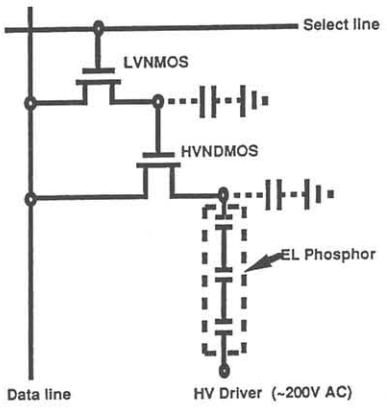


Figure 1. Two Transistor AMEL Pixel Cell

Fig. 2 illustrates pixel operation for an NMOS access device. The 60 Hz field period is sub-divided into a number of separate LOAD and ILLUMINATE sub-periods. During the LOAD cycle, the high-voltage AC is off, the gate of N1 is driven high and the digital data present on the data line is transferred to the gate of N2. The data is dynamically stored on the gate capacitance of N2 when the gate of the access transistor is subsequently driven low. During the ILLUMINATE cycle, the high-voltage AC signal is applied to the pixel electrode, with the select and data lines grounded. The data stored on the

gate of N2 during the previous LOAD cycle determine if the drive transistor is in its conducting or blocking state, and thus whether the EL material is illuminated. If a logic 1, (5V) has been stored, the NDMOS will be in its on state, operating in the linear regime, and essentially the full AC voltage appears across the EL material, causing it to illuminate. If a logic 0 has been stored, the NDMOS is in its blocking state, the voltage appears across the DMOS transistor instead of the EL material, and no illumination occurs.

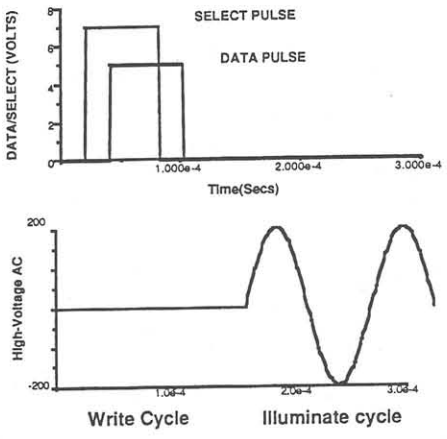


Figure 2. Electrical Operation of the AMEL Pixel Cell

Gray-scale control is achieved, digitally, by time-averaging over each of the individual ILLUMINATE sub-periods. Since all transistors are either fully-on or fully-off, power dissipation within the panel is minimized.

## 4. AMEL Process/Device Technology

The pixel structure shown in Fig. 1 requires an IC technology capable of integrating high-density, high-performance CMOS with high-voltage (>150V) DMOS and which is compatible with a subsequent EL deposition. This has been achieved using a novel, thin-film silicon-on-insulator (SOI) approach. High density is achieved by burying the active circuitry directly beneath the EL material and by and using SOI to provide device isolation in minimum area. The starting material was four-inch diameter ISE™ silicon wafers with a 1μm thick buried oxide and a 1μm thick superficial silicon layer. Mesas were etched to define the individual device islands followed by ion implantation of the n-well, p-well, and DMOS drift regions. Separate implants were required for the drift and n-well regions to allow independent optimization of the CMOS and DMOS devices. A conventional LOCOS process was used to form the 8000Å thick oxide over the DMOS drift region necessary for adequate field shielding. Next, polysilicon was deposited, doped, and patterned to form the device gates. Boron was then implanted and diffused to form the self-aligned DMOS channel in the conventional way. The n+ and p+ source/drains were formed by phosphorus and boron implantation respectively. Next came multi-level interconnect deposition, planarization, and deposition of the EL stack.

The NMOS and PMOS devices resulting from this process exhibit good electrical characteristics, including symmetric (± 1.1V) threshold voltage, low-leakage, good subthreshold characteristics (90mv/dec), high drive current and high electron and hole mobilities (450,220 cm2/Vsec respectively). The DMOS device employs the well-known RESURF principle for high-voltage capability, exhibits low-leakage, and is capable of withstanding up to 220 V. Operation with pixel sizes as small as 24μm x 24μm has been demonstrated, resulting in very high resolution of > 1000 lines/inch.

In summary a novel, high-density, active-matrix, electroluminescent display has been fabricated using single-crystal silicon-on-insulator technology. This new approach offers many advantages including high brightness, superior speed, low power dissipation, high pixel density, high resolution, good gray-scale performance, and improved reliability. Pixel arrays as large as 1280 X 1024 have been successfully fabricated using 24 μm X 24μm pixels.[6)]

## 5. Active Matrix LCD's

The first use of single crystal SOI material in flat panel displays was the fabrication of a 192 X 192 Liquid Crystal Display that was originally designed to be fabricated in polysilicon technology.[1)] Since that time The Sarnoff Center has also been involved in the design of 640 X 480, 1280 X 1024, and 2560 X 2048 displays for projection applications.[7)]

The process for fabricating these displays involves standard silicon on insulator (SOI) technology with the addition of a black matrix deposited on the transistor plate to improve aperture ratio and to eliminate alignment problems with the top plate. The process also includes the addition of light shields to minimize carrier generation due to the high light levels common in projection systems. For the fabrication of small pixels, however, a modification of this process which includes electrical and optical shields is needed. The final structure is shown in figure 3. This structure includes a single crystal silicon layer which is used to form the pixel transistor as well as the silicon electrode.

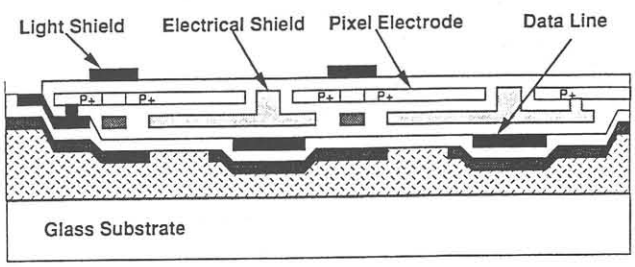


Figure 3. Shielded LCD Pixel Structure

The silicon electrodes are placed as closely together as possible to minimize disclination formation under the data line. There is also a polysilicon layer which is used to form an electrical shield between the data lines and the silicon electrode as well as between the data line and the LC material. This layer is also used to increase the storage capacitance on the pixel and, therefore, is placed completely across the silicon electrode. Figure 4 shows the layout of the 24 μm pixel structure.

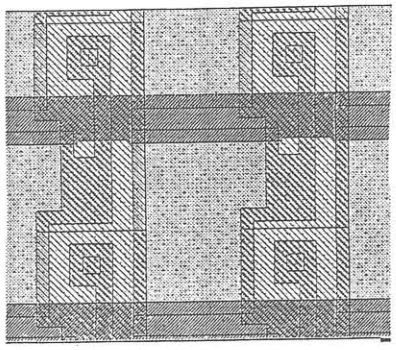

Figure 4. 24 μmX 24μm Pixel with Electrical Shields Between the Data/Select Lines and the Pixel Electrode

This pixel exhibits excellent contrast ratio and no coupling between the data/select lines and the pixel electrode. This pixel also has an integral black matrix which is built into the select and data lines. No additional black matrix level is needed.

Pixels as small as 12μm X 12μm have been fabricated using the shielded pixel concept as shown in figure 5. Such small pixels, however, will also need to incorporate a modified drive technique as the simple column or line inversion technique causes pixel-to-pixel disclinations to be visible.

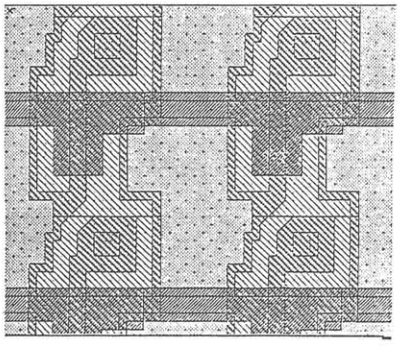

Figure 5. 12μm X 12μm Pixel Shielded Pixel

It is expected that these 12 μm X 12μm pixels will be used to form the next generation of LCD's at the 2048 X 2560 level.

In summary SOI technology is presently being used to fabricate 24 μm pixel structures which will be used in 1280 X 1024 projection displays. These pixel structures incorporate novel layers to increase the aperture ratio and contrast ratio in very high density LCD's for helmet and virtual reality applications. Smaller pixels are also being investigated for use in 2048 X 2560 displays but will require even more sophisticated improvements in structure and drive technique in order to achieve comparable contrast ratio and brightness.

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