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High-Speed 0.5μm SOI 1/8 Frequency Divider with Body-Fixed Structure for Wide Range of Applications

T.Iwamatsu, Y.Yamaguchi, K.Ueda*, K.Mashiko*, Y.Inoue and T.Hirao

*ULSI Laboratory, *System LSI Laboratory, Mitsubishi Electric Corporation*
4-1, Mizuhara Itami City Hyogo, 664 Japan

A High speed SOI 1/8 frequency divider was demonstrated with body-fixed structure using filed-shield(FS) isolation. The maximum operation frequency is 2.1GHz at 3.3V. The SOI divider is about 1.6 times faster than that of the bulk divider with the same dimension. The power consumption of the SOI divider at the maximum operating frequency is about 60% of that of the bulk divider. Inverter characteristics were also improved with body-fixed structure, and it was indicated that the body-fixed SOI structure is able to be applied for analog circuits.

1. Introduction

Recently, demands for low-power LSI's have been much increased for low power systems, such as handy communication systems, used in a forthcoming multimedia era. Thin-film SOI MOSFET's are attractive for low-voltage operation[1]-[3] due to reduced junction capacitance and reduced back-bias effect. So far, various kinds of reports with high-speed and low-power features[4][5], and high-performance circuits[6]-[8] were presented using thin-film SOI devices. In these reports, however, almost all papers treated floating SOI transistors. For the handy systems, stable operation of analog circuits is necessity. For realizing of SOI analog circuits, the floating effect should be eliminated by body-fixed structures.

In the present report we introduced a body-fixed SOI frequency divider using filed-shield isolation technique[9], and obtained stable transistor and inverter characteristics. Using the body-fixed SOI we demonstrated GHz level high speed SOI 1/8 frequency divider whose frequency corresponds to handy communication systems. These results suggest that low-power CMOS/SIMOX devices can replace present ECL circuits used in a handy system, and can contribute power reduction expected in the handy systems.

2. Experimental

CMOS transistors were fabricated using two-level poly-crystalline silicon and two-level aluminum process on standard SIMOX substrate. For isolation process, both of LOCOS and FS were used. N-ploy-Si gate was used for both FS gate and transfer gate. NMOS and PMOS transistors operate at partially and fully depleted conditions, respectively. Tungsten polycide (WSi2/poly-Si) on transfer gate and self-aligned titanium silicide (TiSi2) in the source-drain region were used, respectively.

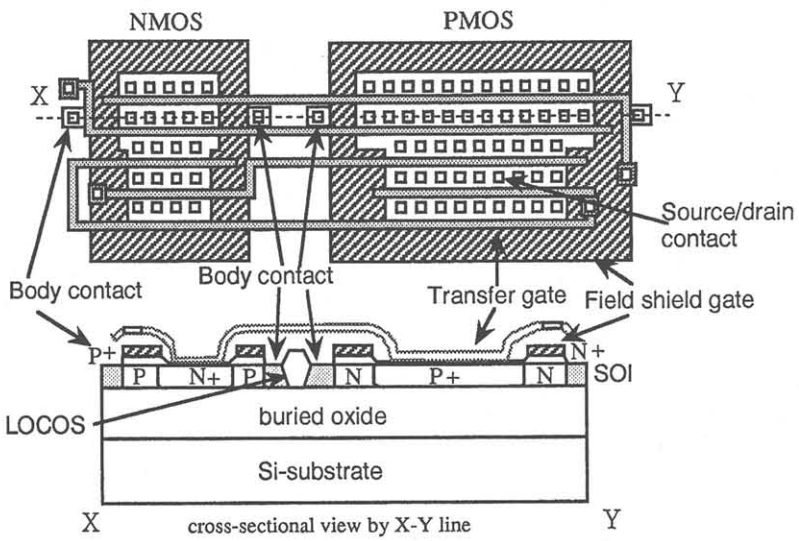

Fig 1. Schematic diagrams of master parts in CMOS/SOI F/F circuits with body-fixed structure using field-shield isolation

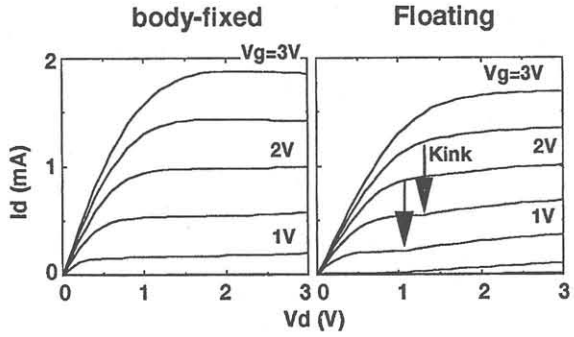

Fig 2. Id-Vd characteristics of the fabricated SOI/MOSFET's L/W=0.5 μ m/4.0 μ m

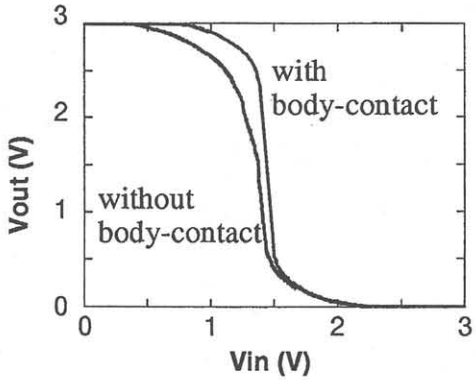

Fig 3. SOI/CMOS inverter characteristics with/ without body-fixed structure

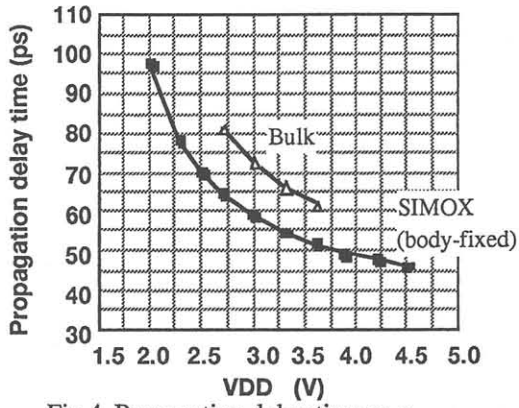

Fig 4. Propagation delay time as a function of Vdd in SOI and bulk ring oscillators (FO=1)

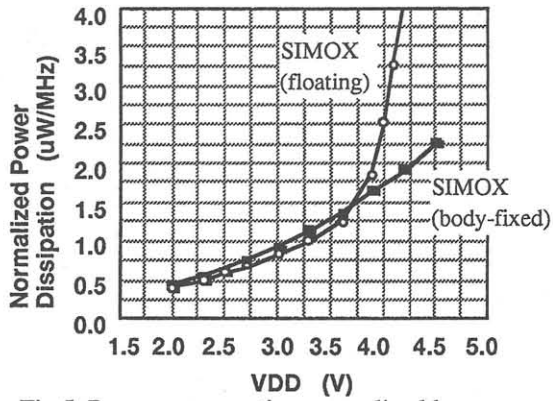

Fig 5. Power consumption normalized by operation frequency in SOI ring oscillators

3. Results and Discussion

Fig.1 shows schematic diagram of a master part of complimentary type flip-flop(F/F) circuits used in the SOI 1/8 frequency divider with body-fixed structure using filed-shield(FS) isolation. LOCOS isolation was used between NMOS and PMOS to avoid latch-up phenomenon and FS gate was formed adjacent between MOSFET's for film contacts. The same CAD system can be used both for bulk and SOI MOSFET's by the FS isolation technique. Well contacts of bulk circuits are used as film contacts for SOI circuits. Id-Vd characteristics from both floating and body-fixed conditions of SOI-NMOSFET's are shown in Fig.2, respectively. In the case of the floating SOI-MOSFET's, the kink effect was observed in saturation region. NMOSFET's operate at the partially depleted condition. The kink in saturation region is caused by the parasitic bipolar action resulting from the accumulated excess carriers in the floating channel. On the other hand, ideal characteristics without floating-substrate effect were obtained in the body-fixed SOI-MOSFET. Inverter characteristics were also degraded by the kink effect, as shown in Fig.3. The linearity in the input-output characteristics was degraded in the floating case. On the contrary the linearity in inverter characteristics was improved with FS isolated structure. From these results, it is suggested that body-fixed SOI structure can be applied for analog circuits.

Fig.4 shows propagation delay time(tpd) in ring oscillators as a function of Vdd. The CMOS ring oscillator consists of 97 stages CMOS inverters in gate array configuration. The body-fixed structure was formed by the FS isolation. The tpd value in the body-fixed SOI ring oscillator was about 80% of those in a bulk Si circuit at Vdd=3.3V. The high-speed operation in SOI devices was achieved by the smaller junction capacitance. Fig.5 shows power consumption as a function of Vdd normalized by operation frequency in the ring oscillator. At high drain voltages, the power consumption in the floating SOI ring oscillator is rapidly increased by BVds lowering due to floating substrate-effect. Whereas in body-fixed SOI, power consumption degradation is not observed at high drain voltages. Because the excess carrier generated near the drain edge is extracted by the body-fixed structure, the channel potential of the body-fixed SOI structure is not increased even in a high drain voltage region. The body-fixed structure is capable of offering 3.3V operation used in conventional bulk circuits even if screening at relatively high voltage is taken account.

The frequency divider is a key component for handy-communication systems. To verify the validity body-fixed structure, we fabricated a 1/8 frequency divider. Circuits composition of a complimentary type F/F circuit

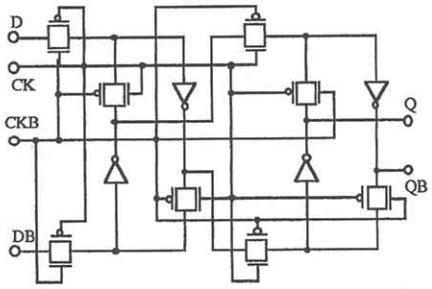

Fig 6. F/F circuit
used in the frequency divider

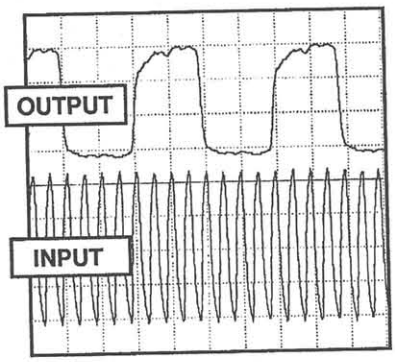

Fig 7. Operating waveform
of the 1/8 frequency divider
: input frequency is 2.1GHz
400mV/division; 1ns/division

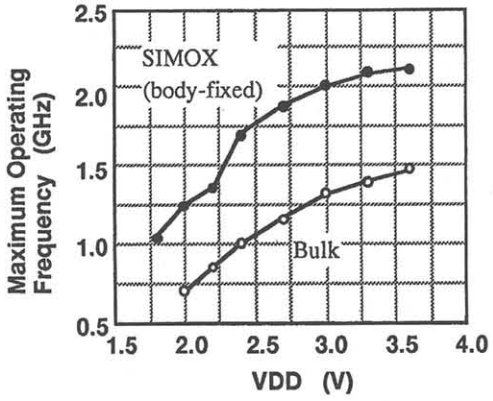

Fig 8. Maximum operating frequency
in SOI and bulk 1/8 frequency dividers

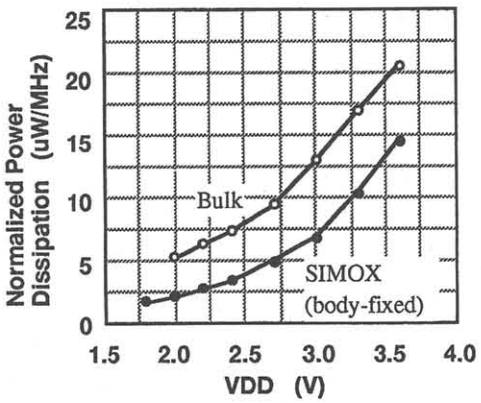

Fig 9. Power dissipation normalized by operation
frequency in the SOI and bulk 1/8 dividers

used in the 1/8 frequency divider is shown in Fig.6. The 1/8 frequency divider operates in a static mode and consists of three serially connected F/F circuits. The operating waveforms at an input frequency of 2.1GHz, which was measured at 3.3V, are shown Fig.7. The power dissipation was 10 μ W/MHz at 3.3V. Fig.8 shows the maximum operation frequency as a function of Vdd for SOI and bulk dividers. The bulk-Si result was calculated by circuit simulation. The frequency of the SOI divider is about 1.6 times faster than that of the bulk divider at 3.3V. The normalized power consumption of the SOI divider at the maximum operating frequency is about 60% of that of the bulk divider as shown in Fig.9. It is suggested that the high-speed and low-power consumption characteristics are due to reduced junction capacitances, and also due to the reduced back-bias effect in the transmission gates.

4. Conclusion

We have fabricated a 1/8 frequency divider on a 0.5 μ m SOI gate array with body-fixed structure using field-shield isolation technique, and demonstrated a maximum operation frequency of 2.1GHz and a power dispassion of 10 μ W/MHz at Vdd=3.3V. The body-fixed structure improved the linearity in inverter characteristics and suppressed kink in Id-Vd characteristics as well as BVds improvement that have been subjects in formerly reported floating SOI devices. By these improvements, SOI application would be expanded even to analog circuits. SOI MOSFET's are potentially attractive for high-speed and low-voltage operation, and hence these results suggest that SOI devices can apply handy system that is expected to be used in a forthcoming multimedia era.

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