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New MOS Current Mode Logic Using SOI-MOSFET with Body Terminal

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New SOI-MCML (MOS Current Mode Logic) circuits have been proposed for the high speed and low voltage application of LSIs. In our new MCML circuits, the body terminals of SOI-MOSFETs are connected to the gates. It has been shown that the operation speed can be significantly increased and the supply voltage can be reduced to less than 1V by using these new circuits.

1. Introduction

Recently, the demand to the high speed and low power LSIs has become rapidly increasing. Therefore, SOI devices which have the capability of high speed and low power operation have attracted great attention again. To lower the supply voltage is the most effective way to reduce the power consumption in LSIs. The threshold voltage must be decreased to improve the current drivability when the supply voltage is lowered. However, the low threshold voltage results in the larger cut-off current. Accordingly, we encounter the trade-off between the current drivability and the cut-off current. However, for the application with a low supply voltage of 1V or less, we can overcome such trade-off problem using SOI-MOSFET with body terminal which is connected with the gate[1][2] because the threshold voltage is decreased only when the high signal voltage is applied to the gate. The SOI film body is forward-biased through the body terminal and the threshold voltage is lowered when the high voltage is applied to the gate because the body terminal is connected with the gate. The current through the forward-biased p-n junction can be low if the bias voltage is less than 1V. The low threshold voltage in the high gate voltage region is very effective to increase the current drivability. On the other hand, the threshold voltage can remain high to reduce the cut-off current in the low gate voltage region. From the viewpoint of high speed circuit, it has been said that a small signal swing is very effective for improving the operation speed. Therefore, MOS current mode logic (MCML)[3] has attracted attention as a high speed circuit with small signal swing.

In this paper, we have proposed a new MCML circuit using SOI-MOSFET with the body terminal which is connected with the gate terminal.

2. Configuration of New SOI-MCML Circuit

A cross-sectional view and a top view of SOI-MOSFET with the body terminal are illustrated in Figure 1. In our new MCML circuit, the body terminal of SOI-MOSFET is connected to the gate. We call such SOI-MOSFET "BCG (Body terminal Connected to Gate) SOI-MOSFET". The subthreshold characteristics are

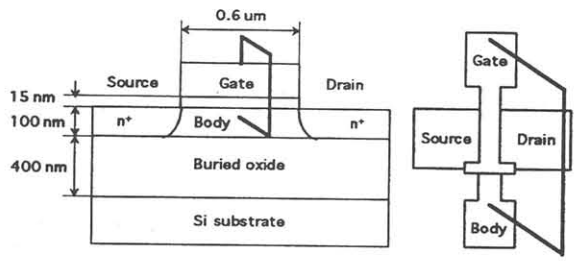

Figure 1: A cross-sectional view and a top view of SOI-MOSFET with the body terminal.

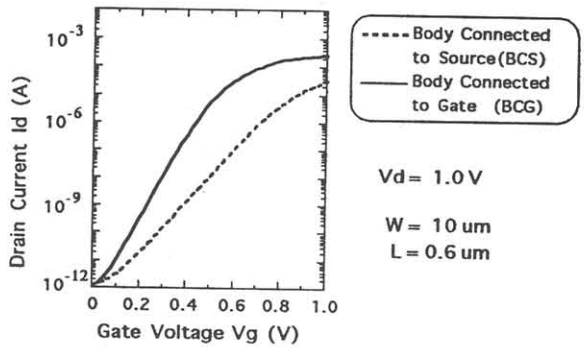

Figure 2: Subthreshold characteristics of SOI-MOSFET.

dramatically improved in BCG SOI-MOSFET when compared with SOI-MOSFETs with floating body or with body terminal which is connected to the source. The threshold voltage can be decreased with no increase of cut-off current in BCG SOI-MOSFET due to the improved subthreshold characteristics as shown in Figure 2. Figure 3 shows a new MCML circuit (BCG SOI-MCML) which we propose. This circuit consists of a pair of BCG SOI-MOSFETs and a constant current source. In this circuit, the threshold voltage of SOI-MOSFET for "high" input signal is lower than that of SOI-MOSFET for "low" input signal. The difference between these threshold voltages can be considered equivalently as the increase of the differential input signal voltage. Therefore, the external differential input signal swing can be reduced in this circuit.

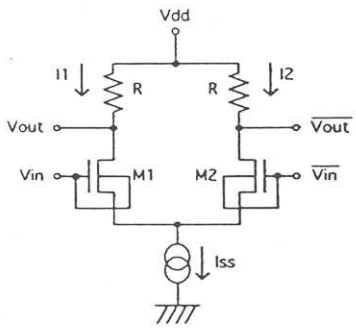

Figure 3: BCG SOI-MCML circuit.

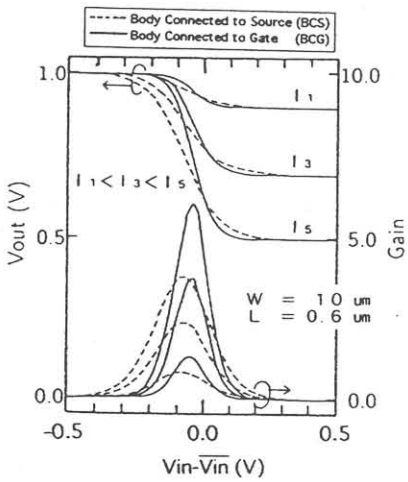

Figure 4: Measured DC transfer characteristics and gain of SOI-MCML as a function of differential input signal voltage.

3. Basic Characteristics of SOI-MCML Circuits

The measured DC transfer characteristics and gain of BCG SOI-MCML are plotted as a function of the differential input signal voltage in Figure 4 where the value of the current source is changed as a parameter. The results of MCML circuit using SOI-MOSFET with the body terminal which is connected to the source (BCS SOI-MCML) are also plotted in the figure for the comparison. As is obvious in the figure, the transfer curves of BCG SOI-MCML show steeper transition compared with those of BCS SOI-MCML and hence the gain of BCG SOI-MCML is considerably larger than that of BCS SOI-MCML. Consequently, the differential input signal swing can be significantly reduced in BCG SOI-MCML. The measured DC transfer characteristics of SOI-MCML are re-plotted as a function of the non-differential input signal voltage Vin in Figure 5 where both output signals are shown. It is obvious in the figure that the full output signal swing is obtained to the input signal swing of 0.2V in BCG SOI-MCML while the full output signal swing is not obtained in BCS SOI-MCML. Thus, the input signal swing can be decreased in BCG SOI-MCML. Therefore, BCG SOI-MCML has the capability of the high speed and low voltage operation.

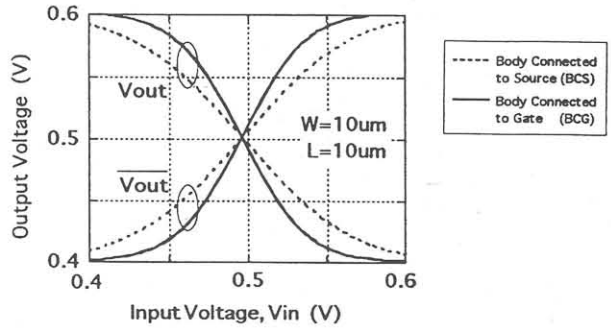

Figure 5: Measured DC transfer characteristics of SOI-MCML as a function of non-differential input signal voltage.

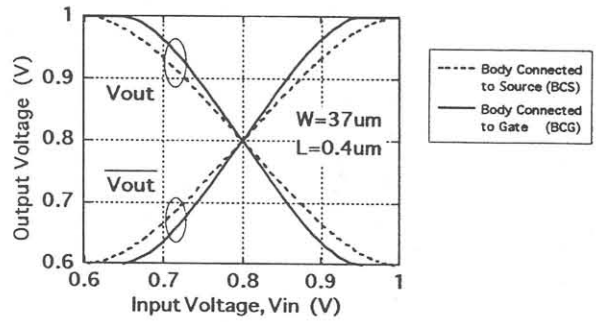

Figure 6: Simulated DC transfer characteristics of SOI-MCML as a function of non-differential input signal voltage.

4. Performance of SOI-MCML Circuit Evaluated by Simulation

The capability of SOI-MCML for the high speed and low voltage operation is investigated in more detail by the circuit simulation. SOI-MOSFETs with smaller size (Lg=0.4um) are used in the simulation. The simulated DC transfer characteristics are shown in Figure 6 where it is clear again that larger output signal swing can be obtained in BCG SOI-MCML. This means that the channel width of SOI-MOSFET can be reduced in BCG SOI-MCML when the identical output signal swing with BCS SOI-MCML output is required. The minimum channel width to maintain the excellent transfer characteristics are plotted as a function of the signal voltage swing in Figure 7. As is obvious in the figure, the channel width in BCG SOI-MCML can be reduced to around 60% of that in BCS SOI-MCML. This also facilitates the high speed operation because the capacitances can be reduced. Figure 8 shows the minimum supply voltage as a function of the signal voltage swing. It is clear in the figure that the minimum supply voltage can be more dramatically reduced in BCG SOI-MCML as the signal voltage swing is decreased.

The input/output waveforms of 10-stage SOI-MCML and SOI-CMOS inverter chains with 100fF load capacitance per each stage are shown in Figure 9 where the input waveforms are indicated by dotted lines and the output waveforms by solid lines. Three kinds of SOI-MCML inverter chains are compared each other in the figure. It is obvious from the figure that BCG SOI-MCML with smaller signal swing represents the highest speed. Figure

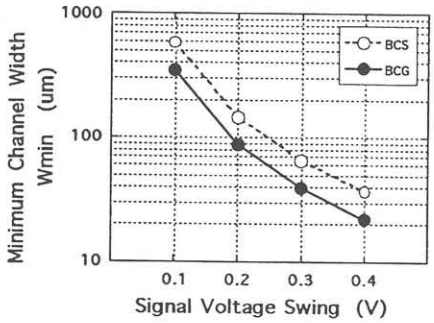

Figure 7: Minimum channel width as a function of signal voltage swing.

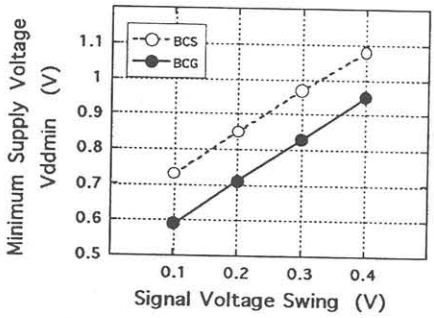

Figure 8: Minimum supply voltage as a function of signal voltage swing (VTO=0.6V).

10 shows the delay time as a function of load capacitance. It is more obvious from the figure that the delay time of BCG SOI-MCML with smaller signal swing increases more slowly as the load capacitance increases and hence BCG SOI-MCML is very suitable for the high speed operation.

For the output buffer, we also propose new latch type SOI-MCML as shown in Figure 11. The body terminal of one SOI-MOSFET is connected to the drain of the other SOI-MOSFET in this MCML. More remarkably steep transition with hysteresis in DC transfer characteristics can be obtained in the latch type SOI-MCML as shown in Figure 12.

5. Conclusion

New SOI-MCML circuits have been proposed for the high speed and low voltage application of LSIs. The body terminals of SOI-MOSFETs are connected to the gates in these circuits. It has been shown that the operation speed can be significantly increased and the supply voltage can be reduced to less than 1V by using these new circuits.

6. Acknowledgment

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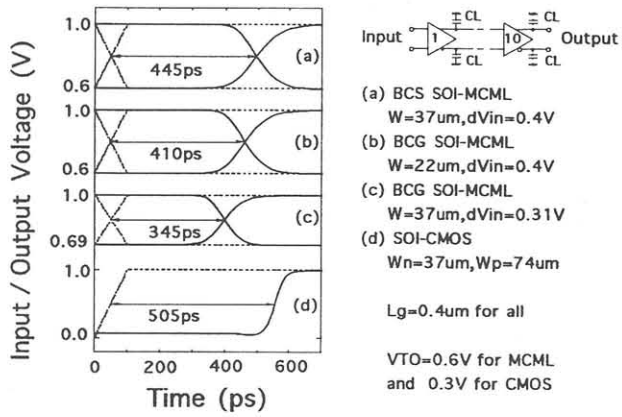

Figure 9: Simulated waveforms of 10-stage inverter chains.

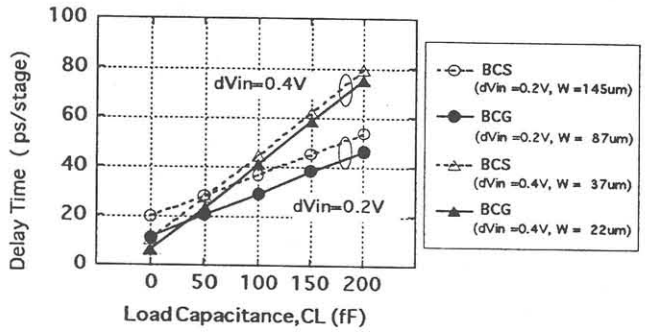

Figure 10: Simulated delay time as a function of load capacitance.

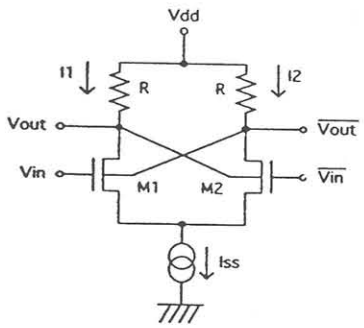

Figure 11: Latch type SOI-MCML circuit.

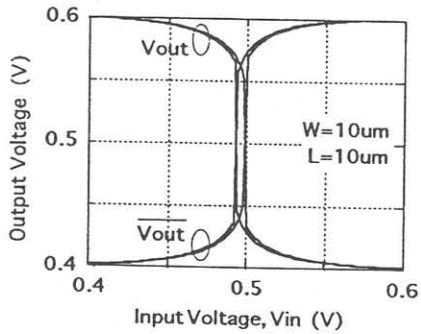

Figure 12: Measured DC transfer characteristics of the latch type SOI-MCML.