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Vth Rolloff Free Sub 0.1 μm SOI MOSFETs Using Counter Doping into a Uniformly and Heavily Doped Channel Region

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[Abstract] We proposed counter doping into a heavily and uniformly doped channel region of SOI MOSFETs, and demonstrated a V_{th} rolloff free 0.075 μm-L_{Geff} nMOSFET. This technology also enables us to obtain a proper threshold voltage V_{th}, and to eliminate parasitic edge-gate or back-gate transistors.

[Introduction] An SOI MOSFET operates at a low power due to its negligible junction capacitance. However, we also require superb short channel immunity with low V_{th}, and we must eliminate edge-gate or back-gate transistors to suppress standby current. Using a thin-film SOI substrate with a thickness t_{Si}, and doping it by ion implantation with a dose of ϕ_B followed by a sufficient thermal process, we can obtain a uniformly and heavily doped substrate with a doping concentration, N_B, of ϕ_B/t_{Si}. We demonstrate that counter doping into this substrate satisfies all above the demands for low-power operation.

[Fabrication Process] Figure 1 shows our proposed device structure. SIMOX substrates with SOI and buried oxide thickness of 100 nm and 400 nm were used.

Boron ions were implanted into SOI substrates through a 15-nm thick SiO_2 layer at 20 keV and a dose of 2×10^{13} cm^{-2}. They were then annealed at 1000°C for 60 min in a dry nitrogen atmosphere, resulting in a uniformly and heavily doped punchthrough stopper. Then, We performed counter doping with Sb for various doses, Φ_D, after removing the oxide layer in order to from a counter doped channel and adjust the V_{th}. A 4-nm-thick gate oxide was produced at 900°C, and the conventional MOSFET process was used. We annealed at 1000°C for 5 s to activate impurities in the source/drain regions. We used Co salicide technology for the gate and source/drain regions to reduce parasitic resistance. Figure 2 shows the cross-sectional TEM image of the fabricated device with a effective gate length of 0.075 μm. $CoSi_2$ was formed completely on gate polysilicon with less than 0.1-μm gate length. SOI layer in source/drain region remained about 300 nm after Co salisaide process. Sheet resistance of source/drain and gate were 6.7 Ω/sq. and 4.7 Ω/sq..

[Results and Discussion] The as-implanted Sb profile is almost shifted parallel after gate oxidation due to silicon consumption, but the profile itself is almost invariable, even after subsequent annealing at 1000°C for 30 s, as shown in Figure 3. This is due to the low diffusion coefficient of Sb in silicon. The B profile is uniform after 1000°C for 60 min of annealing (Figure 3), and the profile is invariable during subsequent annealing, as verified by process simulation. Therefore, the V_{th} of this device is robust and stable if the as-implanted Sb profile is precisely evaluated.

The V_{th} of long-channel devices (L_{eff} = 0.59 μm) is well controlled from 0.8 to 0.2 V with increasing Φ_D, and this is clear from the analytical model derived by solving a one dimensional Poisson equation, as shown in Figure 4.

The low V_{th} necessary for high-speed, low-voltage operation must be accompanied with a reduced short channel effect. Figure 5 shows the dependence of V_{th} on the gate length on various Φ_D. We obtained a low V_{th} of 0.2 V and rolloff free characteristics down to an effective gate length, L_{Geff}, of 0.075 μm using Φ_D of 6.3×10^{12} cm^{-2} and an acceleration energy of 26 keV. If we use a uniform channel doping profile with an N_B of 5×10^{17} cm^{-3} without counter doping, we can adjust V_{th} to 0.3 V, but the V_{th} rolloff in the L_{Geff} is less than 0.2 μm. Consequently, the combination of high and uniform background doping and counter doping overcomes the scaling limit of bulk MOSFETs. Although this technology is not limited to SOI devices, a stable uniform profile is possible with SOI substrates.

In SOI MOSFETs, LOCOS isolation often results in subthreshold leakage due to a lower value of V_{th} on the Si island edges, resulting in a high standby current. The fabricated device showed no "hump" in the subthreshold region, as shown in Figure 6. This indicates a higher value of V_{th} in parasitic transistors. It is attributed to the uniform and high background doping of N_B of about 2×10^{18} cm^{-3}, and means that this technology completely eliminates parasitic transistors without introducing channel cut doping. The subthreshold swing of the device was 90 mV/decade which is mainly determined by background doping and hence is not low for long-channel devices, but its value is independent of gate length.

[Conclusion] We proposed counter doping into a uniformly and heavily doped SOI substrate. We showed that this enables us to adjust proper V_{th} while holding superb short-channel immunity. It also enables us to eliminate parasitic edge-gate or back-gate transistors without introducing channel cut doping. We also showed the channel doping profile is invariable during thermal processing. Therefore, the V_{th} of this device is robust and is accurately estimated by an analytical model. We demonstrated rolloff free V_{th} characteristics down to 0.075 μm L_{Geff} with a value of 0.2 V.

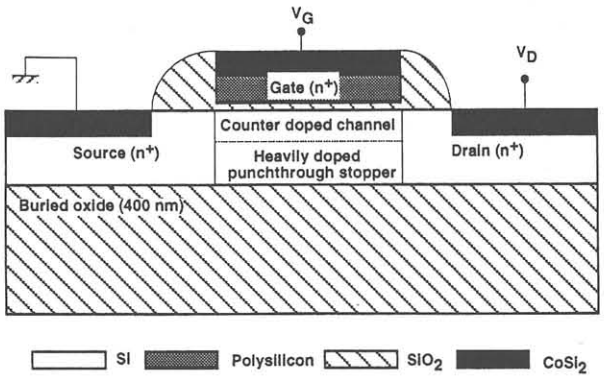

Figure 1. Proposed SOI nMOSFET. The channel region was first highly-implanted with B and subsequently enough annealed, resulting in a uniformly and heavily doped p substrate. Then, counter doping was introduced at the surface region by Sb ion implantation. This MOSFET is a partialy depleted type.

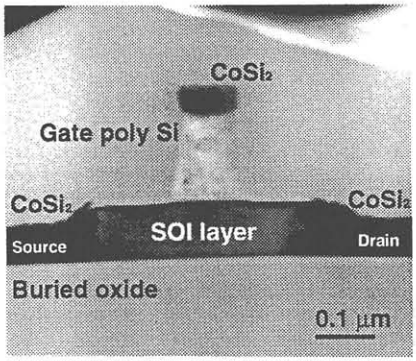

Figure 2. Cross-sectional TEM image of the fabricated device with effective gate length of 0.075 μm.

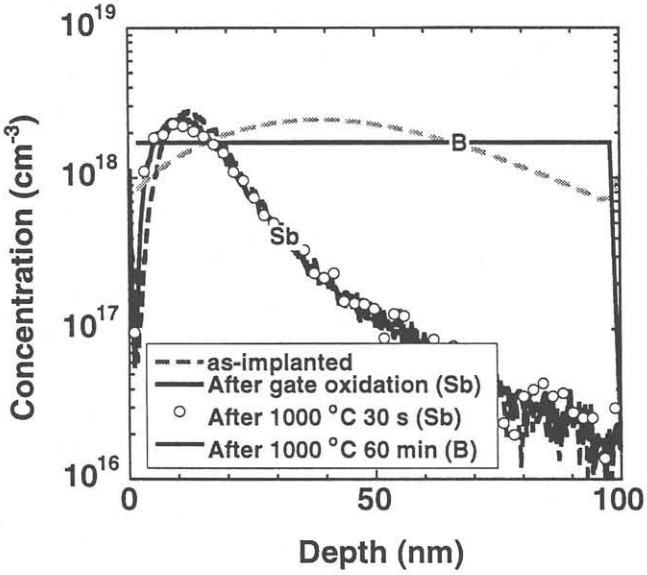

Figure 3. Redistributed profile of counter doped Sb and background doped B. Sb profile was measured with SIMS and B profile was evaluated with a process simulator SUPREM IV. Sb was implanted at 30 keV with a dose of 5 x 10^{12} cm^{-2} .

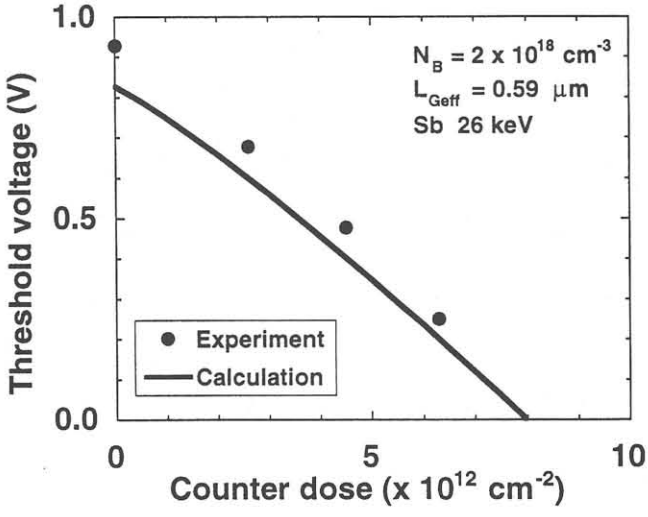

Figure 4. Threshold voltage dependence on counter dose. The calculated values were obtained by solving one dimensional Poisson equation.

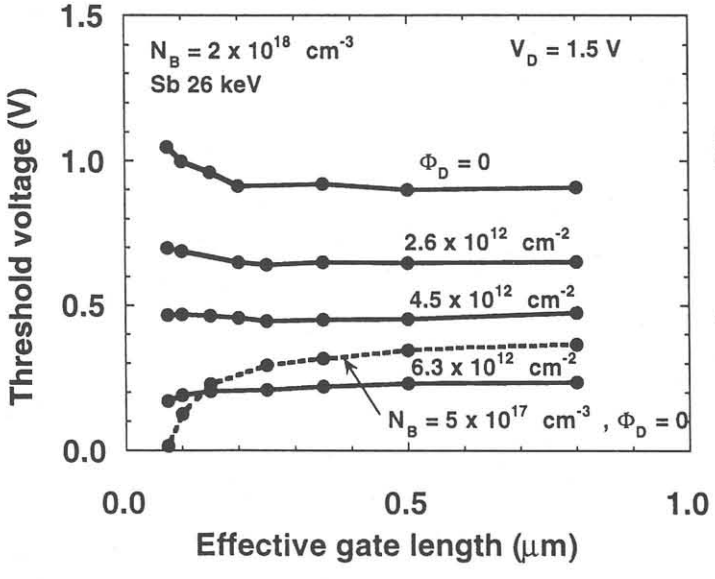

Figure 5. Dependence of threshold voltage on effective gate length with various background doping, N_B, and counter dose, Φ_D.

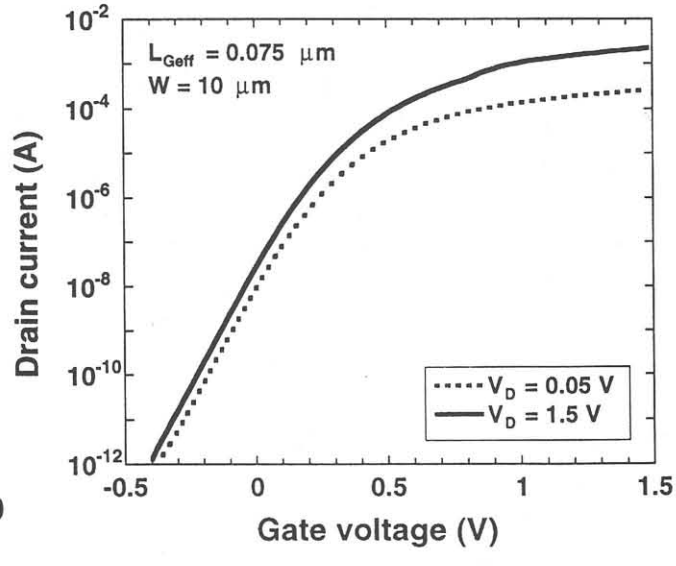

Figure 6. Subthreshold characteristics of 0.075 μm-L_{Geff} device. The subthreshold swing was 90 mV/decade.