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Characterization of SOI Substrates for ULSI Applications

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Characterization methods able to provide the electrical image of SOI materials are reviewed systematically from wafer screening to device-related evaluation. The Ψ–MOSFET and back-gate-controlled transport measurements are suitable for in-situ evaluation of as-grown wafers. Instead of MOS capacitance and conductance measurements, a number of current-based methods are proposed: MOS–Hall profiling, charge pumping, noise spectroscopy, and Zerbst-like transients. Selected experiments are presented and used to update the list of SIMOX properties.

1. INTRODUCTION

Silicon On Insulator (SOI) technology has reached a stage of successful development and is being regarded as an attractive candidate for low voltage ULSI circuits. A major condition for competing with bulk silicon in commercial applications is the quality of starting wafers. Rapid material optimization implies efficient characterization of SOI substrates.

This paper reviews several electrical characterization techniques which are appropriate in SOI since they can overcome the difficulties induced by the film thickness and stacked interfaces. The potential of the *pseudo*–MOS transistor for exploring the properties of as-grown wafers is compared with more or less conventional transport experiments. In fully-processed wafers, MOS transistors stand as an invaluable tool for exploring the properties of the Si film, front-gate oxide, buried oxide, and related interfaces. By contrast to the case of MOS capacitors (more difficult to implement in thin, multi-interface SOI), the drain current is easily measurable even in small area devices. Moreover, the experiment can be conducted separately from the front or back interface in order to probe different regions of the structure. A brief survey of selected methods is given in the context of SIMOX technology.

2. WAFER SCREENING

2.1. Ψ–MOSFET Technique

The pseudo–MOS transistor (Ψ–MOSFET) results from the upside-down MOS structure that is inherent in all SOI materials. Figure 1 shows that the bulk Si substrate acts as a gate terminal and can be biased, through the metal support, to induce a conduction channel at the interface. The buried oxide plays the role of a gate oxide and the Si film represents the transistor body.

To operate *in situ* (without lithography and metallization) the Ψ–MOSFET, low pressure probes are placed on the film and form source and drain point contacts.[1] The basic setup is composed of any two-probe system, connected to a HP–4145 pico-ameter.

According to the positive or negative bias of the gate, accumulation or inversion channels are active at the interface. Very pure subthreshold $I_D(V_G)$, transconductance, and output $I_D(V_D)$ curves are produced. The *threshold and flat-band* voltages are determined from $I_D(V_G)$ characteristics. The inversion region is discriminated from the accumulation region by a larger sensitivity to probe pressure. Increasing the pressure from 10 to 50 g gradually reduces the series resistances and provides accurate carrier mobilities.[2]

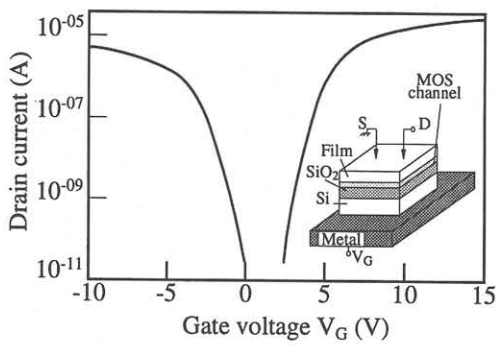

Fig. 1. Pseudo-MOS transistor and typical $I_D(V_G)$ characteristics in a fully depleted SIMOX film.

In order to cancel first order series resistance effects, the values of μ_0 and $V_{T,FB}$ are extracted by plotting the function $I_D/\sqrt{g_m}$ versus V_G. The slope, $\sqrt{f_g \mu_0 C_{ox} V_D}$, yields the mobility for electrons or holes, and the intercept gives V_T or V_{FB}. Due to non-parallel current lines it is not possible to define the width and length of the Ψ–MOSFET. An empirical aspect ratio, $f_g \simeq 0.75$, was determined experimentally.[2]

Doping levels above $5 \times 10^{15} cm^{-3}$ are quite precisely detected. The densities of *fixed charges* in the buried oxide and *interface traps* are extracted, respectively, from the flat-band voltage and subthreshold slope.

2.2. Transport Measurements

In response to intrinsic problems (high sheet resistance, full depletion, in-depth inhomogeneity) and new opportunities (substrate biasing), the transport measurements are more refined in thin film SOI than in bulk Si.

Hall effect in van der Pauw configuration provides basic transport parameters such as resistivity, carrier mobility and concentration, scattering process, etc. The

experiment is used to monitor the optimization of SOI materials, achieved by increasing the carrier mobility and suppressing contamination sources. Varying the substrate bias, as for the Ψ–MOSFET, it is possible to investigate independently the transport properties in the film volume and at the upper interface of the buried oxide. Channel Hall mobilities for electrons and holes are measurable on the same wafer.

The following are more techniques useful for electrical evaluation of unprocessed SOI wafers:[1)]

- Four-point probing of the film resistivity.
- Spreading resistance for in-depth resistivity profiling.
- Nondestructive pinhole detection by decomposition of a $CuSO_2$ solution when a leakage current passes through the buried oxide.
- Surface photovoltage for measuring the diffusion length of minority carriers.
- Photoconductivity for determining the carrier recombination lifetime.
- PICTS (Photo-Induced Current Transient Spectroscopy) for analysis of the deep traps.

3. DEVICE-BASED CHARACTERIZATION

3.1. SIS and MOS Capacitors

The capacitance and conductance techniques, frequently used for extracting the parameters of Si-SiO_2 interface in bulk silicon MOS systems, can still be applied to the SOI capacitor structures. In a silicon-insulator-silicon (SIS) capacitor, the film is biased through a metal contact (gate) and the back of the wafer is grounded.

The conventional MOS capacitor theory and equivalent circuit are modified to account for depletion regions and interface traps on each side of the buried oxide. The problem with SIS capacitors is that there are too many unknown parameters and only part of them can be determined by combining low- and high-frequency measurements. The oxide thickness is deduced from the measured maximum high-frequency capacitance.[1)] Then, the doping concentrations in film and substrate are calculated from the minima of the high-frequency capacitance. The fixed oxide charge is inferred from the voltage shift and the interface trap densities from the stretchout of C-V curves or from the conductance peak. This method becomes rather difficult in thin fully depleted films.

Even more complex is the case of MOS-SOI capacitors where two oxides and three interfaces coexist. A body contact is useful for performing "independent" front- and back-gate measurements. However, the series resistance is responsible for parasitic components.

3.2. In-Depth Profiling

The properties of thin SOI films may vary with distance from the top surface to the buried insulator. In non-uniform films, the average values of resistivity, mobility and autodoping are meaningless, since they may look very poor, even if the properties of the top portion of the layer reaches bulk Si standards. The profiling method combines MOS and transport measurements.

An MOS-Hall device is a depletion-mode MOSFET with several small lateral contacts. Hall effect and magneto-conductance measurements are performed at low drain bias as a function of V_G. By gradually depleting the film, the thickness of the conducting region is reduced and the measured (average) transport properties are modified. A procedure involving differentiation provides the contribution of the infinitesimal layer, situated at the limit between depletion and "active" regions.

3.3. Charge Pumping

Charge pumping (CP) provides the concentrations of interface traps. The adaptation of CP to SOI requires a contact to the Si film: either 5–terminal MOSFETs or gate-controlled p-i-n diodes may be used.[3)] The gate is repeatedly switched from inversion (where minority carriers are trapped on the interface states) to accumulation (where the trapped carriers recombine with majority carriers). The carrier recombination gives rise to a charge pumping current I_{CP} in the substrate terminal, which is a frequency-amplified measure of the trap density.

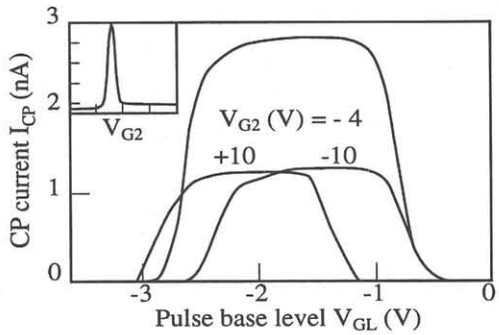

Fig. 2. Front gate CP current versus pulse base level for various back gate voltages.

A very meaningful CP curve (Fig.2) is obtained by varying the bottom level of the trapezoidal pulse while keeping the pulse magnitude and frequency fixed. A "rectangular" curve is obtained: the left and right edges yield the threshold and flat-band voltages, whereas the plateau level gives the trap concentration.

Shown in Fig.2 is the modification of the CP signature by interface coupling as the back interface goes from inversion to depletion and accumulation. It follows that for the front interface traps to be accurately characterized, the back gate has to be maintained in strong inversion or accumulation.

3.4. Low-Frequency Noise

The $1/f$ noise of MOS transistors originates from fluctuations in the carrier number due to tunneling between the inversion channel and slow oxide traps. Figure 3 shows the typical variation of the $1/f$ noise factor, S_I/I_D^2, from the weak inversion "plateau" to the strong inversion slope. The density of slow traps is calculated from the plateau level. If many deep-level impurities

are present, the $1/f$ noise changes in a recombination-generation $1/f^2$ spectrum. The interface coupling impacts on noise measurements in two main respects: noise generation at the opposite interface and modification of the surface potential by the opposite gate bias.[1)]

In very small area devices, the trapping of one carrier can easily be detected in the time domain as a small pulse superimposed on the average current. The duration of this Random Telegraph Signal (RTS) gives the time constant of the trap, whereas the pulse magnitude depends on oxide thickness. The back channel of SOI MOSFETs is an ideal tool for studying the properties of RTS fluctuations because C_{ox} is very small and allows larger pulses to be obtained.

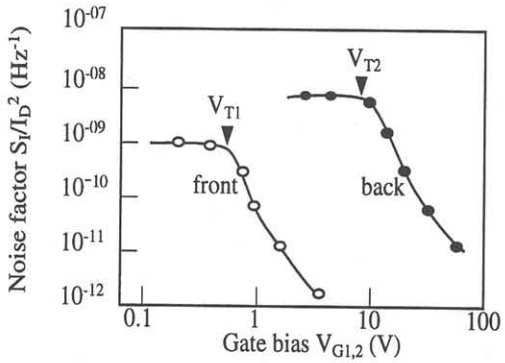

Fig. 3. Normalized $1/f$ noise factor versus gate voltage.

3.5. Drain Current Transients

The drain current transients are exclusive SOI techniques, imagined to exploit the special dual-gate configuration of SOI transistors. In floating-body, enhancement-mode SOI MOSFETs, there is no source of majority carriers, except the generation process. The experiment is designed to induce a deficit of holes: the front gate is biased in strong inversion, whereas the back gate is pulsed from depletion to accumulation. The holes requested in the accumulation layer are released from the neutral region of the film. A deep depletion region forms under the gate and the film potential drops. To maintain front gate charge conservation, the excess depletion charge is compensated by a temporary drop in the inversion charge. The current relaxes back to equilibrium through carrier generation within the film and at the interfaces.[1)]

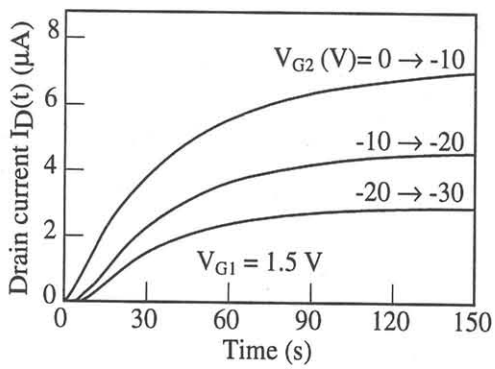

Fig. 4. Drain current transients in a SIMOX n–MOSFET.

The current transient is monitored with a HP-4145 system and appropriate models provide the generation rates. Note that similar experiments may be performed on accumulation-mode SOI MOSFETs.

4. TYPICAL PROPERTIES IN SIMOX

The SIMOX film is stress-free. Dominant defects are threading dislocations (10^5–$10^6\,cm^{-2}$ in standard SIMOX, only 10^2–$10^4\,cm^{-2}$ in multi-implanted or low-dose SIMOX) and small stacking faults ($10^6\,cm^{-2}$). No obvious electrical activation of dislocations is visible for concentrations below $10^6\,cm^{-2}$. Film contamination from implanter, furnace or capping layers has drastically been alleviated. An intrinsic source of contamination of SIMOX films is due to subsisting oxygen atoms, which give rise to *thermal donors*. The original p-type conductivity of the starting Si wafer is converted to n-type.

Our Ψ–MOSFET and van der Pauw measurements indicate that the residual doping level of commercially available SIMOX wafers is low enough (2–$5\times10^{15}\,cm^{-3}$, slightly higher in multi-implanted SIMOX). Typical Hall mobilities are rated from 800 to $1200\,cm^2V^{-1}s^{-1}$ in the film and up to $600\,cm^2V^{-1}s^{-1}$ at the buried interface. The carrier scattering mechanisms are comparable with the case of bulk Si. The minority carrier lifetime may exceed $100\,\mu s$. This demonstrates the excellent crystal quality as well as its in-depth homogeneity.

The buried oxide differs from a thermal oxide: it is Si-rich which explains the high density of electron traps (strained Si-Si bonds) and E' centers (acting as hole traps). Slow traps have equally been observed. The breakdown field exceeds 8 MV/cm. Localized defects (silicon pipes) may cause accidental leakage current. Crystalline Si inclusions in the bottom of the oxide, reduce its effective thickness and hardness. Lateral fluctuations of the film and oxide thickness are below 5 nm.

The interfaces are sharp. The density of traps and fixed charges at the upper interface of the buried oxide is typically in the range of 0.5–$2\times10^{11}\,cm^{-2}eV^{-1}$. It is definitely larger than at the gate oxide interface but small enough not to adversely affect the circuit performance.

5. CONCLUSION

Selected characterization methods, especially conceived for SOI or imported from bulk silicon, have been revisited and used to reveal the electrical image of SIMOX. The silicon film is device-grade, wafer-scale monocrystal with high quality and excellent electrical properties. This promotes SIMOX as the most suitable technology for thin-film CMOS circuits.

1) S. Cristoloveanu, S.S. Li, *Electrical Characterization of Silicon-On-Insulator Materials and Devices*, Kluwer Acad. Publ. (1995).

2) S. Cristoloveanu, S. Williams, IEEE Electron Device Lett. **13** (1992) 102.

3) T. Ouisse et al, IEEE Trans. Electron Devices **38** (1991) 1432.