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A High Performance 0.05μm MOSFET with Thin SOI/Buried Oxide Structure

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A high transconductance 0.05 μm NMOSFET has been realized by using thin SOI / buried oxide structures. The measured and the intrinsic transconductance values amount to 472 mS/mm and 702 mS/mm, respectively. We have demonstrated for the first time that the electron velocity amounts to the saturation velocity in SOI structures. However, the transconductance in SOI MOSFETs was reduced by the self-heating effect. Therefore, it is important to suppress the self-heating in order to realize a high speed SOI MOSFET using the carrier velocity overshoot.

1. INTRODUCTION

Since the carrier velocity in MOSFETs is saturated in the stationary equilibrium, the transconductance does not increase in spite of scaling the their dimensions down. Therefore, the realization of the velocity overshoot or the ballistic transport phenomenon [1,2] is considered to be a key factor in realizing a high speed sub-0.1 μm device. A thin film SOI device has an advantage in suppressing short channel effects and realizing high mobility. In the application of SOI devices, however, the self-heating effect is enhanced by decreasing SOI thickness, t_{SOI}, or increasing buried oxide thickness, t_{BOX} [3,4], and enhances the degradation of the device performance.

In this paper, we will demonstrate a high performance 0.05 μm MOSFET with thin SOI / buried oxide structure, and show that the electron velocity is nearly equal to the saturation velocity, considering the self-heating.

2. EXPERIMENTAL

A 0.05 μm NMOSFET was fabricated in a 30 nm thick SOI on an SIMOX wafer with a thin buried oxide layer having thickness, t_{BOX} = 80 nm. The device have n^+ polycrystalline silicon gates and non-LDD source/drain structures. The impurity concentration in the channel is less than 1×10^{16} cm^{-3}. The gate oxide thickness was 4 nm. Electron beam lithography was used to form ultra short gate electrodes. The average channel temperature increment due to self-heating was measured by the gate-electrode-resistance method [3]. Back gate bias of -4 to -8 V was applied to suppress the short-channel effect.

3. RESULTS AND DISCUSSION

The 0.05 μm device shows good drain-current characteristics as shown in Fig. 1.

Figure 2 shows the measured transconductance, *Gm*, at Vd = 1.5 V, versus the effective channel length, L_{eff} . *Gm* value of the 0.05 μm MOSFET amounts to 472 mS/mm. Figure 2 also shows the intrinsic transconductance, *Gmi*, considering the parasitic resistance, where the effective channel length is derived by Terada's method [5]. Here, the parasitic resistance is the sheet resistance of the source region, and is 700 $\Omega\mu$m in this device. The obtained *Gmi* of a 0.05 μm device was 702 mS/mm.

In order to understand how the self-heating affects *Gmi*, we studied the behavior of *Gmi* against drain bias. In Fig. 3 (a) and (b), the dependence of *Gmi* in an SOI MOSFET on the gate drive is compared with that in a bulk MOSFET. In this measurement, the drain bias is varied from 1 to 2 V. *Gmi* of the bulk MOSFET increases with increasing the drain bias because the lateral electric field increases. In case of the SOI MOSFET, however, decrease of *Gmi* is observed. A possible explanation is as follows. As the drain bias increases, the device power also increases. As a result, the self-heating effect is enhanced. Therefore, *Gmi* decrease occurs.

In order to confirm the above assumption, we measured the channel temperature of the SOI MOSFET by the gate-electrode-resistance method. Figure 4 shows the channel temperature versus the device power, where the channel length is 0.1 μm. Since the heat capacity of the thin film SOI is very small, the SOI temperature is uniform throughout the channel region. This is also verified by the heat transfer simulation. In Fig. 4, it is shown that the 0.05 μ m MOSFET channel temperature under *Gm*-max bias increases by over 45K compared with the room temperature.

On the other hand, it is well-known that the saturation velocity, v_{sat} , in the bulk silicon decreases when the channel temperature increases. Figure 5 shows the channel temperature versus the calculated v_{sat} using the formula

$$v_{sat} = \sqrt{\frac{8 < E_p >}{3 \pi m_0}},$$

$$<E_p> = E_p \tanh(\frac{E_p}{2kT}),$$

where, $<E_p>$ and E_p are the average optical-phonon energy and the optical-phonon energy [6]. Since the buried oxide is very thin, *i.e.* t_{BOX} = 80 nm, the self-heating is suppressed. Therefore, the increment of the channel temperature is estimated to be about one half that of the device with t_{BOX} = 300 nm [3]. However, shown as Fig. 4, the channel temperature amounts 335 K at the measurement condition of *Gm*-max at L_{eff} = 0.05 μm. As shown Fig. 5, it is found that v_{sat} for this L_{eff} is reduced to be 8.7×10^6 cm/sec.

Here, we estimate measured the velocity overshoot over the calculated saturation velocity shown in Fig. 5 the *Gmi*, as shown in Fig. 6. It is newly found that the ratio of the electron velocity to the saturation velocity, v/v_{sat} at L_{eff} = 0.05 μm is nearly equal to unity, *i.e.* the electron velocity approaches the saturation velocity. However, we could not observe the velocity overshoot even in 0.05 μm devices, while the simulation considering the energy-transport model shows the velocity overshoot at the source region in less than 0.1 μm device.

The substrate bias (from -4 V to -8 V) causes the increase of the effective transverse field, E_{eff}. When the absolute value of the back gate is very small, it is considered that the back gate interface scattering increases. However, figure 7 shows that the transconductance is independent of the back gate bias, which indicates that both the back gate oxide interface state and E_{eff} do not affect the electron velocity. Therefore, the reason why the carrier velocity does not overshoot the bulk saturation velocity is considered as follows. The self-heating probably decreases the energy relaxation time, or the saturation velocity in the inversion layer decreases, in comparison with the bulk saturation velocity [7].

4. CONCLUSION

High transconductance 0.05 μ m NMOSFETs have been realized by using thin SOI / buried oxide structures. The measured and the intrinsic transconductance values amount to 472 mS/mm and 702 mS/mm, respectively. We have demonstrated for the first time that the electron velocity amounts to the saturation velocity in SOI structures. Therefore, even in sub-0.1 μ m region, it is important to miniaturize the MOSFET dimensions to realize a high speed device. However, we cannot observe the velocity overshoot even in 0.05 μm . In order to realize a velocity overshoot devices, however, it is necessary to suppress the self-heating effect by reducing the buried oxide thickness in a thin SOI structure.

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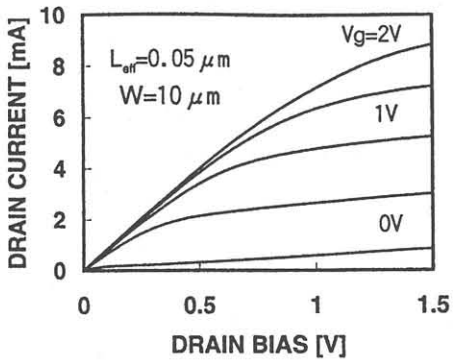

Fig. 1. Drain current of L_{eff} = 0.05 μm, where V_{sub} = -4V.

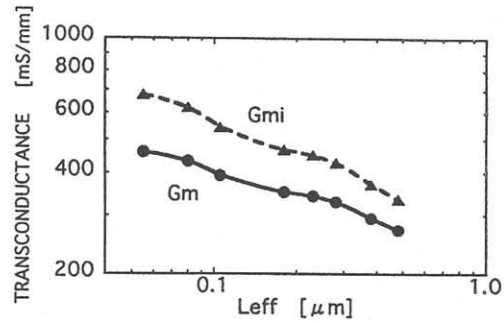

Fig. 2. L_{eff} dependence of the measured transconductance, *Gm*, at V_d = 1.5 V. It also shows "intrinsic" transconductance, *Gmi*. Closed circles show *Gm*, and triangles *Gmi*.

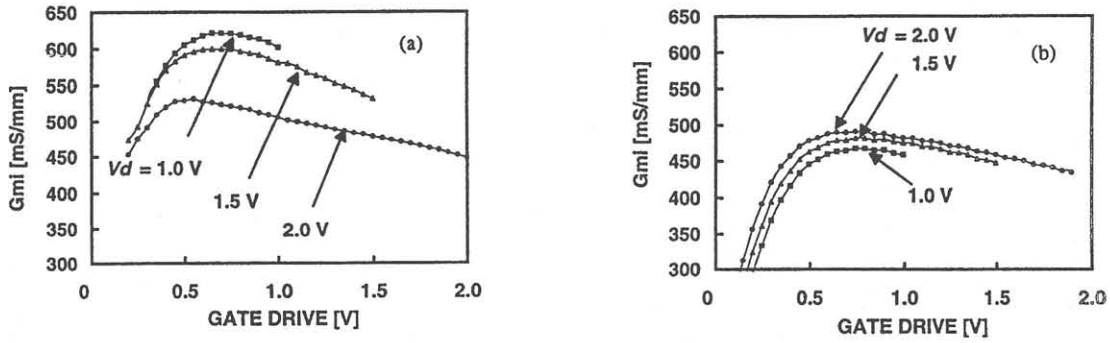

Fig. 3. (a) shows the dependence of *Gmi* in an SOI MOSFET on the gate drive. (b) shows that in a bulk MOSFET. L_{eff} for both samples is 0.13 μm. Increasing the drain bias, *Gmi* decrease in the case of the SOI MOSFET, (a), while increases in the case of the bulk MOSFET, (b).

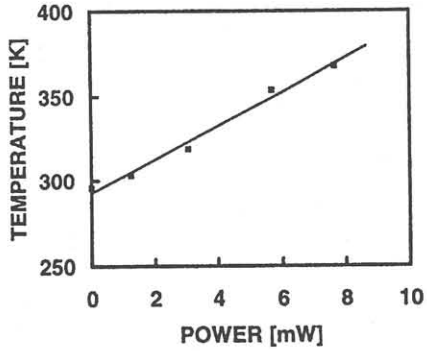

Fig. 4 Power dependence of the channel temperature. it is shown that the 0.05 μm MOSFET channel temperature under *Gm*-max bias (4.5 mW) increases by over 45K compared with the room temperature.

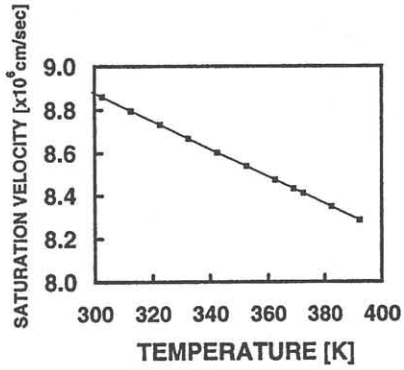

Fig. 5 Temperature dependence of the bulk saturation electron velocity, v_{sat}. The saturation velocity is calculated by the relation between v_{sat} and the average optical-phonon energy [6].

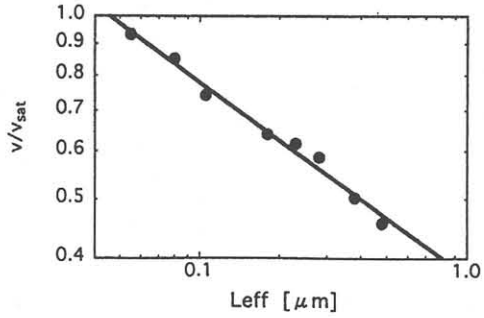

Fig. 6. L_{eff} dependence of v/v_{sat}. It amounts to unity at L_{eff} = 0.05 μm.

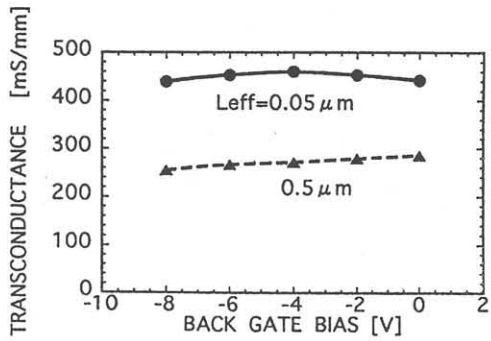

Fig. 7. Back gate bias dependence of the transconductance of 0.05 μ m and 0.5 μ m effective channel lengths, where V_d = 1.5V.