## Two-Dimensionally Confined Carrier Injection Phenomena in Sub-10-nm-Thick SOI Insulated-Gate pn-Junction Devices

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This paper describes two-dimensionally confined carrier injection phenomena in thin-SOI insulated-gate pn-junction devices fabricated on SIMOX substrates. At 28 K, conductance shows step-like anomalies due to the manifestation of a twodimensional subband system for a low cathode bias in an 8-nm-thick-SOI structure. Conductance also shows an oscillation-like feature for a high cathode bias due to the injection mode change. These effects are examined by theoretical simulations based on quantum mechanics.

#### 1. Introduction

The author proposed a new device with an insulated gate pn-junction structure 14 years ago . Generally speaking, bipolar devices do not operate at low temperatures because of a lack of minority carriers. However, since free the insulated gate can induce any type of carrier, the insulated gate structure is a good candidate for bipolar device applications. Recently, quantum mechanical effects in ultrathin MOSFET's/SOI have been studied by some researchers  $^{2-4}$ , but there have been no reports of those effects in pnjunction devices in spite of their importance for future applications.

This paper describes fundamental properties of thin-SOI insulated-gate pn-junction devices at low temperature. Two-dimensionally confined effects on carrier injection are discussed based on the low-temperature characteristics. These effects are examined by theoretical simulations. Finally, possible influences on characteristics of ultrathin MOSFET/SOI devices are mentioned.

#### 2. Experiments

A schematic device structure<sup>1)</sup> and a measurement configuration are shown in Fig. 1. Devices with a 16- $\mu$ m-wide gate and a 7-nm-thick gate oxide were fabricated on the SIMOX substrate with an 8-nm-thick superficial silicon layer (t<sub>s</sub>) and an 80-nm-thick buried oxide layer<sup>4</sup>. Gate length (L) is

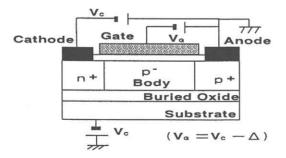


Fig. 1. Schematic device structure and measurement configuration. Reformed geometry for cathode-common configuration. Note that the effective substrate bias exists so as to assist the front gate bias. Gate bias is deeper than the cathode bias by  $\Delta$ .

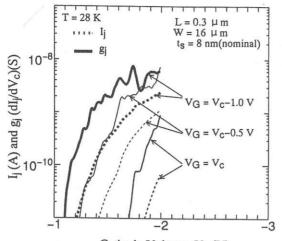
0.3 µm. The p-type body has a doping concentration  $(N_A)$  of  $1 \times 10^{17}$  cm<sup>-3</sup>. An extremely thin SOI structure was used in the expectation of the manifestation of <u>two</u>-dimensional <u>subband</u> system (2DSS)<sup>4</sup>. The measurements were carried out from 300K to 28K.

Junction current  $(I_j)$  and  $g_j$   $(dI_j/dV_c)$ dependences on cathode voltage  $(V_c)$  measured at 28 K are shown in Fig. 2. At 28 K, the  $I_j$  curves show distinct kinks and the  $g_j$  curves show clear step-like features for a low negative  $V_c$  and oscillation-like features for a high negative  $V_c$ . Not only the cathode voltage, but also the gate voltage  $(V_G)$  is swept simultaneously at this configuration, the change in the gate bias results in the Fermi level shift. Therefore the enhancement of the step-like feature probably originates from the effective substrate bias, which assists the front gate bias as shown in Fig.  $1^3$ .

## 3. Physical models and simulations 3-1. Fundamental models

Simple schematic band diagrams of the device operation are shown in Fig. 3. Here, the of the local impurity influence sites is neglected. Fig. 3(a) shows the carrier injection mechanism for a low negative  $V_{\rm G}$  and Fig. 3(b) shows that for a high negative  $V_{\rm G}$ . Since a whole SOI layer is 8-nm thick, the 2DSS must be created over the whole SOI layer. Since the transition region of the pn junction is thin, the region is also quantized. Even in the transition region, carriers must show the two-dimensional (2-D)transport nature. Carriers transit between discrete levels by the spatial extent of relevant wave functions. This scheme is almost the same as the three-dimensional (3-D) case fundamentally and is acceptable for the dc analysis.

In Fig. 3(a) for a low negative  $V_G$ , lots of electrons still exist even at high energy levels in the n<sup>+</sup> region. In this case, electron injection from the n<sup>+</sup> to the p<sup>-</sup> region might be possible because the electron concentration in the p<sup>-</sup> region is not so low. In Fig. 3(b) for a high negative  $V_G$ , on the other hand, many holes exist even at high energy levels in the p<sup>-</sup> region because the hole Fermi level incidentally goes down beneath the valence band top, which results in the decrease in electron concentration in the p<sup>-</sup> region. In contrast, in the n<sup>+</sup> region, the



Cathode Voltage, Vc (V)

Fig. 2. Forward junction current  $(I_j)$  and channel conductance  $(g_j)$  dependences on cathode voltage at 28 K. Absolute values are plotted for  $g_j$  values.

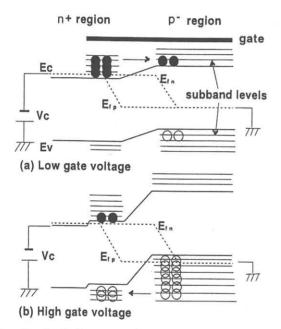


Fig. 3. Band diagrams in the device under the two different gate voltage conditions.  $E_c$ : conduction band bottom  $E_v$ : valence band top  $E_{fp}$ : the Fermi level of holes  $E_{fn}$ : the Fermi level of electrons

electron Fermi level goes down below the conduction band bottom, which results in a relative increase in the hole concentration. Therefore, the previous electron injection is suppressed and the hole injection from the p to n<sup>+</sup> region is strongly promoted. The above experimental results suggest each injection mode is ruled by the 2-D subband levels and the density of states of each carrier type, and that  $g_j$ directly reflects the 2-D subband structure.

#### 3-2. Theoretical simulations

The above experimental results are examined by a simplified theoretical model, where a plain rectangular potential well, a low-injection level

and a single subband system for each carrier are assumed for simplicity. Thus, at the lowinjection level, I<sub>j</sub> can be written as

$$I_{j}=I_{j0}[exp(qV_{c}/nkT)-1], \qquad (1)$$

$$I_{10} = qD_p p(V_G) / L_p + qD_n n(V_G) / L_n, \qquad (2)$$

where  $I_{10}$  is the saturation current density,  $D_p$  is the hole diffusion constant,  $D_n$  the electron diffusion constant,  $L_p$  is the hole diffusion length, and  $L_n$  is the electron diffusion length. Diffusion constants were determined from the specific mobility values based on the Einstein relation. The index n is the ideal factor.  $p(V_G)$ and  $n(V_G)$  are the hole and electron concentrations depending on  $V_G$ , respectively. These parameters also depend on the band structure of the 2DSS. In such a thin-SOI system, the potential difference between the top surface potential and the bottom surface potential of the superficial silicon layer is very small. Hence, the top surface potential can be used as a representative of the internal potential. Thus  $p(V_G)$  and  $n(V_G)$  are expressed approximately as

$$p(V_G) = (n_{iq}^2/n_{SOI}) exp(-q\phi_{sn}/kT),$$
 (3)

$$n(V_{\rm G}) = (n_{1q}^2/p_{\rm SOI}) \exp(q \phi_{\rm Sp}/kT), \qquad (4)$$

where  $n_{iq}$  is the intrinsic carrier concentration for the 2DSS,  $n_{SOI}$  is the electron concentration in the n<sup>+</sup> region at the thermal equilibrium,  $p_{SOI}$ is the hole concentration in the p<sup>-</sup> region,  $\mathscr{O}_{Sn}$ and  $\mathscr{O}_{Sp}$  are top surface potentials depending on  $V_G$ . In the practical calculation, the Fermi level  $(E_F)$  and  $n_{iq}$  must be derived. A schematic band diagram for the 2DSS is shown in Fig. 4. From mathematical manipulations, those are given as

$$n_{ig} = \{kT(D_{osn}D_{osp})^{1/2}/t_s\}exp[-E_{C}^*/2kT],$$
 (5)

$$E_{F} = (E_{p1} + E_{a})/2 + (kT/2) \ln[N_{A}t_{s}/D_{osp}kTq],$$
 (6)

$$E_{G}^{*}=E_{p1}-E_{n1},$$
 (7)

where  $\rm D_{OSD}$  and  $\rm D_{OSD}$  are the density of states for electrons and holes, respectively

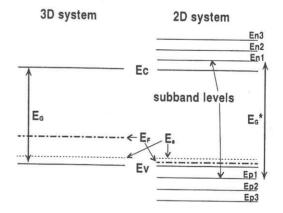
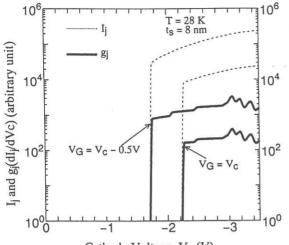


Fig. 4. Schematic band diagram of the twodimensional subband system in a thin-SOI structure compared with the three dimensional system.

 $E_a$ : impurity energy level (acceptors)  $E_F$ : the Fermi energy level  $E_{ni}$ ,  $E_{pi}$ : subband levels



Cathode Voltage, Vc (V)

Fig. 5. Simulated characteristic curves at low temperature. Absolute values are plotted for  $g_m$  and  $g_j$  values.  $I_j$  and  $g_j$  dependences on  $V_c$  for two different gate biases.

Simulated I<sub>j</sub> and g<sub>j</sub> dependences on V<sub>c</sub> for the cathode-common configuration are shown in Fig. 5 at 28 K for the two different gate biases. Step-like features can be seen in the g<sub>j</sub> curves for a low negative V<sub>c</sub> and oscillation-like features are apparent for a high negative V<sub>c</sub>. Since the gate bias is swept with the cathode voltage in this configuration, the Fermi level in the p<sup>-</sup> region is also swept. Hence, the steps in the g<sub>j</sub> curves are also related to the 2DSS at low temperature.

The steps in the  $g_j$  curves are attributed to the hole injection from the  $p^-$  region to  $n^+$  region. Since holes share the subband levels in both the p region and the n region when  $V_{\rm C}$  increases toward the negative direction, the density of injected holes reflects the band structure of the 2DSS. The oscillation-like features for the high negative  $V_c$  are the results of a slightly complicated mechanism. First, the hole injection into the n<sup>+</sup> region becomes dominant for the high negative  $V_c$  (i.e. the high negative  $v_{G'}$ fundamentally, because the concentration of holes injected into the n<sup>+</sup> region is proportional to the concentration of holes sharing subband-level sites the n<sup>+</sup> region. Second, since the hole in concentration is controlled by both the pn product and the charge neutrality in the thin-SOI system, the increase rate of the holes is incidentally affected by the decrease rate of the electron density especially in the n<sup>+</sup> region. In other words, the increase rate of the holes is limited by the decrease rate of the electrons for the high negative Vc. I; characteristics in the insulatedgate pn-junction device are controlled at the same time by both the above factors. This is why the curves have such complicated features. g<sub>j</sub> curves have such completeness Simulation results indicate that the model can explain experimental results well.

# 3-3. Influences on characteristics of extremely thin-SOI MOSFET devices

The most important influence will appear on the parasitic <u>b</u>ipolar <u>action</u> (PBA). The PBA is based on the double injection at the source junction. When the thin-SOI layer is two-dimensionally quantized, the effective density of states decreases<sup>2</sup>). Furthermore, the transport property of either type of carrier is affected by the other through the pn product because of the quantization. In case of thin MOSFET's/SOI. the above two physical mechanisms lead to the suppression of carrier injection across the source junction, which results in the suppression of PBA. Another effect will also assist the suppression of PBA. The 2-D quantization of thin-SOI layer leads to the increase in the effective band gap. This suppresses not only the carrier injection, but also the impact ionization. Thus, it can be expected that the breakdown voltage in extremely thin MOSFET/SOI devices is moderately improved.

#### 4. Conclusion

This paper has described two-dimensionally confined effects on carrier injection phenomena in thin-SOI insulated-gate pn-junction devices fabricated on SIMOX substrates. At 28 K, the conductance shows step-like anomalies due to the manifestation of 2DSS at a low cathode bias in an 8-nm-thick-SOI structure. Conductance also shows an oscillation-like feature for a high cathode bias due to the injection mode change. These influences examined fundamentally were by theoretical simulations based on quantum mechanics.

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