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Process Technology of Bonded SOI Wafers: Recent Development and Quality

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Bonded SOI wafers have many advantages, especially for devices requiring thick SOI active layers. However, the conventional process technology of bonded SOI wafers is found to have a limitation on SOI thickness uniformity for devices such as CMOS requiring 0.1~0.2μm thick SOI active layers. The plasma assisted chemical etching (PACE) method and several etch-stop methods have been proposed to improve the thickness uniformity of bonded SOI wafers. We evaluated these methods and the quality created by them.

1. INTRODUCTION

As easily imagined through the bonding process, the crystallinity of active silicon layers and the insulation of buried oxides of bonded SOI wafers are as good as that of bulk silicon and thermal oxides, respectively. The heavy metal contamination level is similarly controlled to that of bulk silicon. Manufacturing flexibility free from wafer diameter, buried oxide thickness, and the upper limit of the SOI active layer thickness is also the advantage of bonded SOI wafers.[1] On the contrary, the quality of the bonded interface is potentially a shortcoming. The effect of the bonded interface is minimized by placing the bonded interface in the other side of active SOI layers. Therefore, bonded SOI wafers have been widely used except for CMOS application.

In CMOS application, 0.1μm or thinner SOI layers are required with +/-5% thickness uniformity for the fully depletion mode. Even for the partial depletion mode, approximately 0.2μm SOI layers with +/-10% thickness uniformity in a wafer are required.[2] However, because one side of the bonded pair is usually thinned down by grinding and polishing, the SOI thickness uniformity is +/-0.5 ~ +/-0.3μm in a wafer. Thus, in order for bonded SOI wafers to become useful for CMOS application, thinning methods other than polishing have to br developed. One method is to correct SOI thickness variation generated by conventional thinning process with etching or polishing only specified areas. The plasma assisted chemical etching (PACE) technology[3] is one of them. The other method is to transfer an uniform silicon film which is already created on one of the bonded pair prior to bonding. The idea is realized by etch-stop methods.

In this paper, these two different approach methods are reviewed and their quality is evaluated.

2. PACE TECHNOLOGY

The plasma assisted chemical etching (PACE) technology for SOI application was proposed by P. B. Mumola.[3] PACE is the method to improve upon the thickness and uniformity of bonded SOI wafers that have been previously thinned to 1~5μm by conventional methods. As shown in Fig.1, a chemical etching area is confined only under a small electrode where plasma is generated. The size of the electrode is 7~50mm in diameter. The etching rate under the electrode is 10~50μm/min. Before etching, an SOI film thickness is measured by the spectral reflectance method. Because a two dimensional CCD array with 512 x 512 pixels is used, the complete map of the SOI film thickness in a whole wafer is obtained within a couple of minutes. However, only some parts of pixels, such as 64 x 64 pixels out of 512 x 512 are used in measurement, the area resolution of measurement is 2~5mm depending on a wafer size. Based on the SOI thickness map, SOI wafers with high thickness tolerance are locally etched by controlling the position of wafers and the dwelling time for etching.

2.1. Thickness uniformity

Thickness uniformity of SOI films was significantly improved by PACE. After the PACE process, 0.1μm SOI layers in average with a standard deviation of 3nm in a wafer was achieved. Wafer-to-wafer reproducibility was also stable. However, the standard deviation of 3nm in a wafer is not competitive to that of SIMOX wafers. To examine the cause of this SOI thickness tolerance, SOI thickness distribution in a wafer radius direction was evaluated by using the photolithography process and the stylus. As shown in Fig.2, the peak of the SOI thickness appeared every 3~20mm. This indicated that the surface morphology generated by polishing remained even after the PACE. Besides total thickness variation (TTV) of wafers, surface morphology with 10~20nm of peak-to-valley usually appears on polished wafer surfaces with 3~20mm areal wave length depending on polishing methods. For these two parameters determining the shape of silicon wafers, the PACE technology was able to reform the TTV but not able to correct this surface morphology. It is probably because the peak-to-valley pitch was smaller than the PACE electrode. For bonded SOI wafers with less surface morphology, the standard deviation of the SOI film thickness in a wafer was improved to 1.6nm after the PACE process. Thus, for improving the SOI thickness uniformity, the surface morphology is very important.

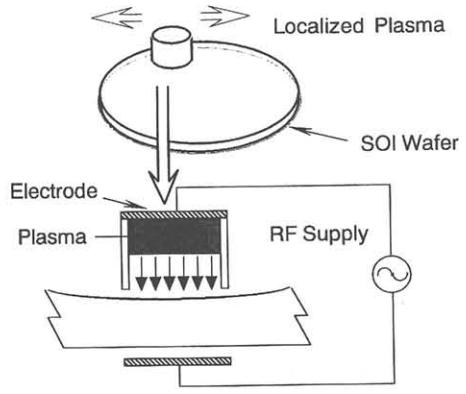

Fig.1. Plasma Assisted Chemical Etching (PACE)
A wafer is scanned in X and Y axis direction beneath a plasma electrode to realize localized chemical etching on a desired area.

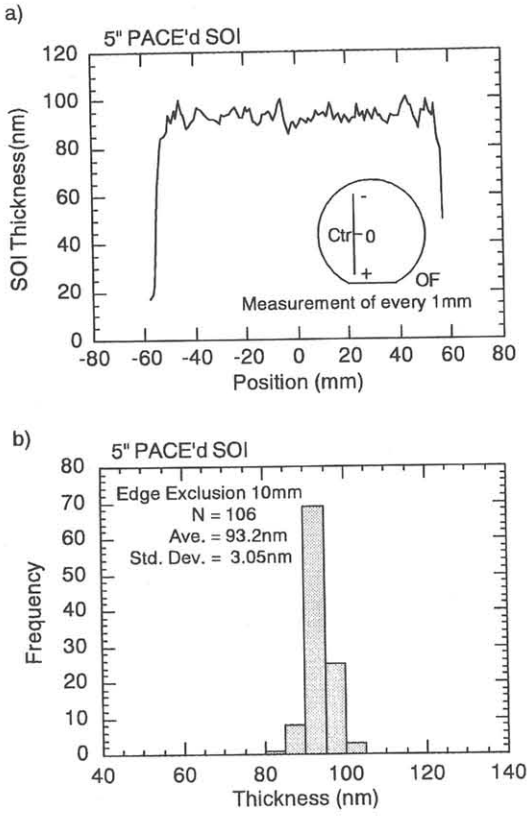

Fig. 2. SOI film thickness distribution (a) in a wafer radius direction and (b) its histogram, measured every one millimeter

2.2. Crystal quality

Bonded SOI wafers are believed to have defect-free active layers based on bulk wafer quality. However, after PACE treatment, the crystal quality of SOI films may be changed. The SOI layer thickness after PACE was 0.1μm, which was too thin for selective etching such as Secco etching for <100> material to evaluate the crystal defects. Thus, we deposited 10μm thick epitaxial layers by chemical vapor deposition (CVD) on 0.1μm bonded SOI wafers thinned by PACE. Then, the deposited epi layers were selectively etched by Secco etching with 1~2μm removal. The samples were observed by optical microscope. For comparison, SIMOX wafers were also evaluated by the same way.

On SIMOX wafers, dislocations with approximately 300/cm^2 in density were observed. On the other hand, bonded SOI wafers had only etch pits with a deformed arrow shape instead of dislocations with a square shape as seen in SIMOX wafers. The density of pits were less than 10/cm^2. Crystal defects associated with these pits could not be detected in this thin SOI layer by TEM. It appeared that crystal quality on bonded SOI wafers after PACE still remained in the bulk silicon level. However, recently, Sadana et al.[4] reported the fairly large number of defects, called nano-voids, found in 0.1μm bonded SOI wafers by the wet selective etching method. We tried the same evaluation and found that the results were not consistent. The pits detected by this method did not even show whether they were crystal defects or not. This kind of crystal quality evaluation was just started.

2.3. Heavy metal contamination

Heavy metal contamination on SOI surfaces treated by PACE was evaluated by Total Reflection X-Ray Fluorescence (TRXF) analysis. The PACE process consists of the PACE itself for thinning SOI layers, slight polishing to recover the degradation of surface quality, and cleaning. When the TRXF analysis was applied to every step, it was found that Cu, Zn, and Fe were detected on surfaces right after PACE. However, these elements disappeared after the slight polishing process as if these elements were wiped off. After cleaning, any contamination was not detected. In conclusion, as long as SOI wafers through the PACE process were cleaned by SC-1 and SC-2, the heavy metal contamination was consistently under detection limit.

2.4. Particles/Protrusions

At the beginning stage of the PACE development, hundreds of protrusions due to particles were observed. Particles dropped on SOI surfaces prior to PACE etching played a role of a mask and prevented from etching SOI layers under the particles. The height of large protrusions was identical to the removed SOI thickness by etching. Particles were said to cause the pipes in buried oxide of SIMOX wafers. Particles are fatal for both bonded SOI wafers by PACE and SIMOX. Recently, the protrusions were reduced to 20~50/wafer, after the particle level in the surrounding

atmosphere was controlled. The slight polishing after the PACE process also helped to reduce small protrusions as well as to improve surface roughness, for which this slight polishing process is effective to SIMOX wafers.

Though the quality evaluation is under consideration in almost every item, the PACE process definitely allows us to obtain 0.1μm or even thinner SOI layers with desirable thickness uniformity. The most advantageous point in this technology is that the conventional bonding technology is basically applicable without modification and that the PACE technology supplements the key drawback of conventional bonded SOI wafers.

3. ETCH-STOP METHODS

SOI layer thickness uniformity produced by etch-stop methods is basically independent of both surface morphology and TTV of original wafers. The SOI active layers created after bonding are formed prior to bonding by either epitaxial growth, diffusion or implantation and are transferred by bonding and etching. Thus, prior to bonding, the formation of new layers which become SOI layers after bonding and the low temperature bonding anneal are required in addition to the conventional bonding process. To stop etching silicon layers with KOH or other alkaline etchants, highly doped boron layers are usually used. There are two methods in etch-stop; the double etch-stop method and single etch-stop method. Due to relatively better final SOI thickness uniformity, the double etch-stop[5] shown in Fig.3 has been used as a popular method. However, this method needs low temperature process (800C or lower) for both bonding anneal and double epitaxial growth. The low temperature bonding anneal may generate delamination of SOI layers.

Recently two notable single etch-stop methods were proposed. One is the boron diffusion method[6] proposed by K. Imai. The growth of double epitaxial layers in the double etch-stop method is replaced by boron diffusion only. This process simplicity implies the reduction of the process cost. The final thickness uniformity depends on the uniformity of boron diffusion in a wafer. Another issue to be developed is how to reduce the boron concentration from active SOI layers after forming SOI structures. The other notable method is the epitaxial layer transfer, called ELTRAN, proposed by Yonehara.[7] In place of highly doped boron layers, porous silicon layers are utilized. Because HF etching selectivity of porous silicon vs. single crystal silicon is over 10^5, the SOI active layer remains as it was formed. At present, hundreds of stacking faults were detected on active SOI layers. The defects may be decreased by preparing a better condition of porous silicon surfaces prior to epi deposition. Besides for SOI fabrication application, because the porous silicon releases the stress at the bonded interface, it is very effective to bond materials other than silicon, such as quartz, on silicon.

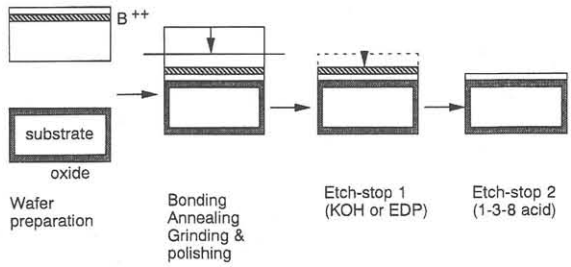

Fig.3. Double etch-stop process flow for creating 0.1μm bonded SOI layers

4. CONCLUSION

The drawback of bonded wafers is the limited active layer thickness uniformity. In place of this conventional polishing process, noble methods, such as the PACE technology and etch-stop methods, were introduced in this paper. SOI wafers through the PACE process were found to have 0.1μm SOI active layers in average and showed the potential of industrial manufacturability with this method due to good reproducibility though the final uniformity was still associated with the surface morphology of SOI wafers prior to PACE process. For etch-stop methods, bonded interface needs to be studied further.

In spite of the short development history of bonded wafers, the bonded SOI technology steadily catches up with desired quality.

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