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Surface Reaction Controlled W-CVD Technology for 0.1-μm Low-Resistive, Encroachment-Free CMOS-FET Applications

Yoshitaka Nakamura, Nobuyoshi Kobayashi, Digh Hisamoto*, Kazunori Umeda* and Ryo Nagai

Semiconductor Development Center, Semiconductor & Integrated Circuits Div., Hitachi, Ltd.
** Central Research Laboratory, Hitachi, Ltd.*
1-280 Higashi-Koigakubo, Kokubunji-shi, Tokyo 185, Japan

A reliable and manufacturable tungsten (W)-stacked source/drain (S/D)-and-gate technology has been developed which is applicable to conventional 0.1-µm CMOS-FETs. A low resistive (2-3 Ω/sq.) and encroachment-free S/D has been achieved. This technology has overcome two major problems in W-CVD: First, the difference in the thickness of W films grown on p^+ and n^+ Si is reduced by Si-light-etching treatment. Second, encroachment is suppressed by a WF_6 high-pressure process. Using this technology, excellent electrical characteristics have been obtained in 0.1-µm CMOS-FETs.

1. Introduction

In scaled CMOS devices, the salicide process has been widely used to lower the S/D and gate resistance. However, the increased resistance in narrow lines and Si consumption caused by silicidation reactions are major concerns for future applications [1]. Recently, a W-stacked S/D-and-gate structure technology has been developed for CMOS-FETs on silicon-on-insulator (SOI) substrates, as an alternative to the salicide technique [2, 3].

In this paper, we propose a W-stacked S/D technique which can be applied to conventional 0.1-µm CMOS-FETs. This technique overcomes two major problems in selective W-CVD: a difference in the growth thickness of W films on p^+ and n^+ Si, and Si consumption during W-CVD (i.e., encroachment). We have developed a reliable W-CVD process for mass production by concentrating on precisely controlling the surface reactions of W-CVD to overcome these problems.

2. Key Technologies for W-CVD

2.1 Difference in Growth Thickness of W on p^+ and n^+ Si

It is well-known that deposited W is thinner on p^+ Si than on n^+ Si [4]. This growth difference depends on the W-deposition temperature; that is, the difference is larger at low temperatures. We found that the difference is also influenced by the MOS-fabrication process used. To investigate the mechanism of this problem, samples A, B, and C were prepared (Fig. 1). The SiO_2 film deposition and etching (CHF_3 plasma) correspond to the gate side-wall spacer fabrication process. After the resist removal and dipping into 0.5% HF, the W films were selectively deposited on the S/D and gate by the reaction of SiH_4 and WF_6 (deposition temperature = 240-280°C, pressure = 10 mTorr).

As a result, a W film with good morphology was grown on the n^+ Si (Fig. 2, A-n^+), while only hemispherical W nuclei were grown on the p^+ Si (Fig. 2,

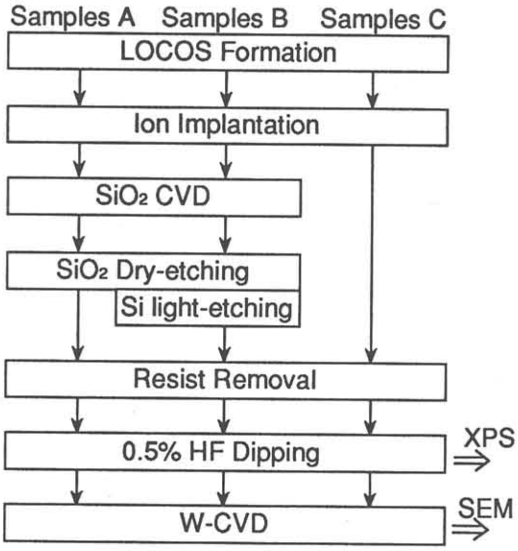

Fig. 1 Schematic process flow after LOCOS formation.

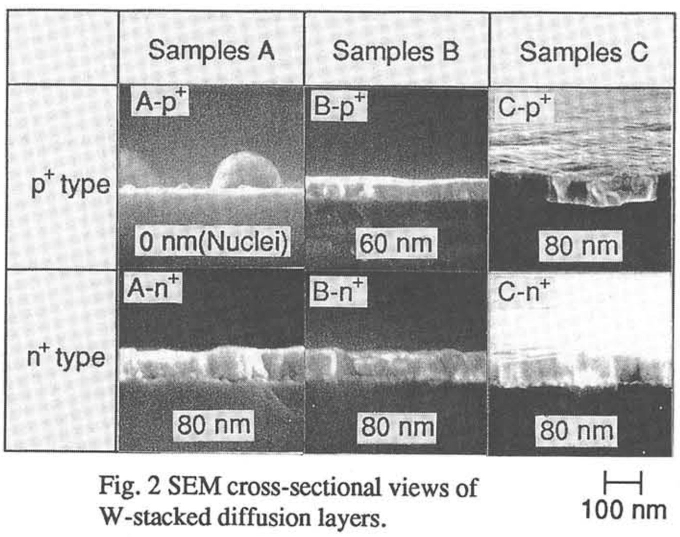

Fig. 2 SEM cross-sectional views of W-stacked diffusion layers.

A-p+). The growth difference was evidently caused by the spacer fabrication process, because 80-nm-thick W films were grown on both p^+ and n^+ Si without that process (Fig. 2, C-p^+ and C-n^+). X-ray photoelectron spectrometry (XPS) analysis showed 5-nm-thick contaminated layers on the Si surfaces of samples A. These contaminated layers contained Si-O, Si-F, Si-C bonds (samples A in Fig. 3). The contaminated layers appear to be the main cause of the growth difference in the W films; however, the thickness and contents of the contaminated layers were exactly the same for both the p^+ and n^+ Si. Thus we think the mechanism of the growth difference is as follows: The contaminated layer prevents WF_6 molecules from adsorbing to the Si surface, reducing the WF_6 concentration on the Si surface, so that the reaction of WF_6 and Si is suppressed. In this case, the density of W nucleation is more influenced by the electronegativity of Si than by the W-deposition temperature. Therefore, the density of W nucleation is much smaller on the p^+ Si than on the n^+ Si.

Based on these results, Si light-etching treatment by CF_4/O_2 downflow-plasma was applied to samples B which were etched approximately 10 nm deep through the Si layer. The thickness of the contaminated layers was thus reduced on the Si surface (samples B in Fig. 3), compared with that of samples A. As shown in Fig. 2, B-p^+ and B-n^+, the growth difference was significantly reduced by the Si light-etching treatment.

2.2 Encroachment

The W-deposition temperature is a key parameter that determines the sheet resistance of W-deposited diffusion layers and the encroachment (Fig. 4). When the W-deposition temperature was low, the resistance was high because the W films contain Si [5]. Additionally, the sheet resistance of the p-type diffusion layer drastically increased at the W-deposition temperatures because the deposited W films were thinner. The encroachment is caused by etching of Si by WF_6 during W-CVD, and this etching reaction strongly increases with the W-deposition temperature, especially on n^+ Si. It is difficult to reduce the encroachment by controlling the W-deposition temperature while also keeping the resistance low.

Thus we have developed a WF_6 high-pressure process. The encroachment was successfully reduced by increasing the partial pressure of WF_6 from 5 to 40 mTorr (Fig. 4(b)). Figures 5(a) and (b) show TEM cross-sectional views of LOCOS edges of n-type diffusion layers with W films deposited at 260°C. The encroachment was only 10 nm with the WF_6 high pressure process (Fig. 5(a)) while the encroachment was 40 nm without it (Fig. 5(b)). An increase in the W nucleation density in the WF_6 high-pressure process is thought to decrease the encroachment.

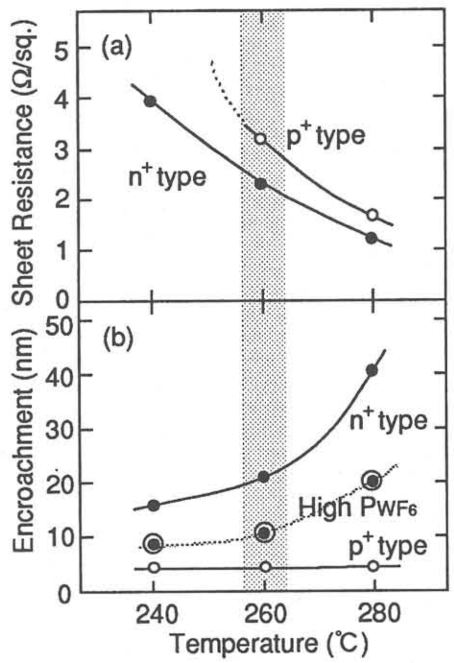

Fig. 4 Sheet resistance of diffusion layers (a) and encroachment (b) as a function of the W deposition temperature.

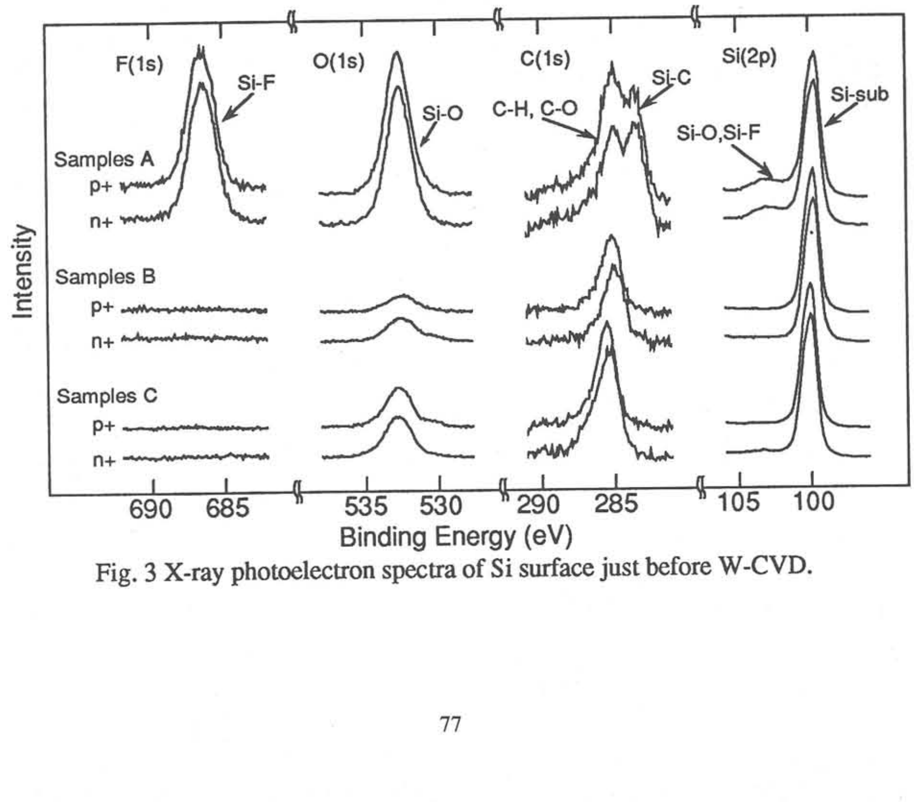

Fig. 3 X-ray photoelectron spectra of Si surface just before W-CVD.

3. Electrical Characteristics of W-stacked CMOS

This W-stacked S/D-and-gate process was applied to 0.1-µm CMOS-FETs. Figure 6 shows an SEM view of CMOS-FETs with W films stacked on the S/D-and-gate. Neither gate-S/D bridging nor selectivity loss in W-CVD were observed in the pMOSs or the nMOSs. The leakage current of the S/D junctions (Fig. 7) and the sub-threshold characteristics (Fig. 8) of the CMOS-FETs were excellent, and high-speed CMOS operation was demonstrated using 0.1-µm CMOS ring oscillators.

4. Conclusions

A feasible technique for fabricating a W-stacked S/D-and-gate structure was demonstrated. The encroachment-free and low resistive (2-3 Ω/sq.) diffusion layers were achieved by precisely controlling the W-CVD surface reactions. This technique is promising for future mass production of 0.1-µm CMOS ULSIs because of its process simplicity and compatibility with the conventional process.

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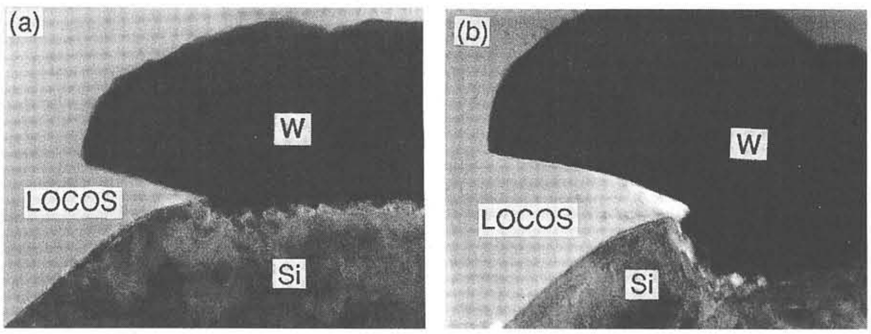

Fig. 5 TEM cross-sectional views of W-stacked diffusion layers: (a) with, and (b) without the WF6 high pressure process. 10 nm

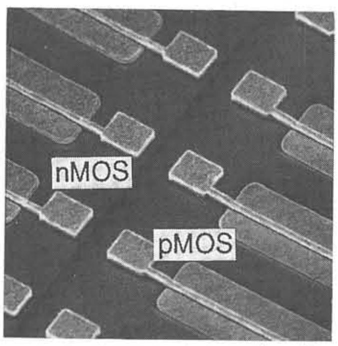

Fig. 6 SEM view of CMOS-FETs. 2 µm

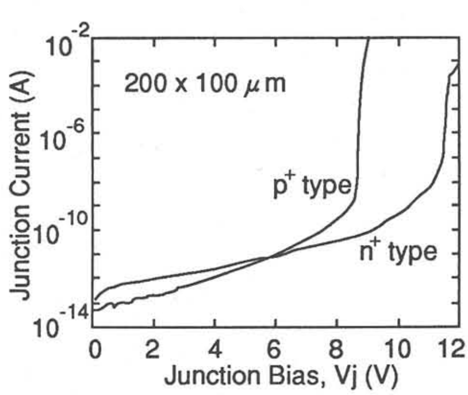

Fig. 7 Junction I-V characteristics.

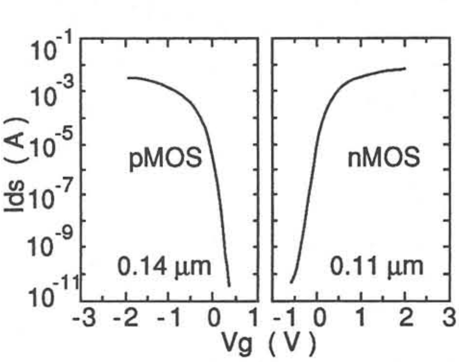

Fig. 8 Subthreshold characteristics of a pMOS-FET and an nMOS-FET: (Tox = 3.5 nm, VDS = 1.5 V).