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W as a BIT Line Interconnection in COB Structured DRAM and Feasible Diffusion Barrier Layer

Jeong Soo Byun, Jun Ki Kim, Jin Won Park, and Jae Jeong Kim

ULSI Laboratory of LG Semicon Co. Ltd., 1, Hyangjeong-dong, Cheongju-si 360-480, Korea

Formation of TiN/$TiSi_2$ bilayer from TiN_X and its utilization as a diffusion barrier for the W bit-line process in capacitor on bit-line (COB) structured DRAM have been discussed in this paper. Since the thickness of $TiSi_2$ formed on Si substrate is very thin and uniform, the TiN_X contacted n^- and n^+ junction revealed good electrical priperties. The compact structure of the overlying TiN enabled the TiN_X to be used as a diffusion barrier for the W process.

1. INTRODUCTION

As decreasing the design rule in DRAM technology, COB structure is more preferred because of its higher packing density compared with capacitor under bit-line (CUB). In general, a CVD WSi_X/*n*-poly (polycide) has been used as the bit-line in COB DRAM. Due to the high resistivity (larger than 100 μΩ · cm) and the polarity (i.e., *n*-type) of the poly-Si, however, it is favoured to replace the polycide by a metal, such as CVD W, for improving the device operation and simplification of fabrication process. In COB DRAM process, the bit-line formation is followed by processes with severe thermal budget (as high as 850℃). Such a thermal process would bring about the destruction of the pre-existing pn junction by forming excessive tungsten silicide (WSi_2).[1] Therefore, for the W bit-line interconnection to be more attractive in VLSI technology, it is highly desirable that a diffusion barrier formed between the W and the Si surface must not only be reliable and stable, but also provide low contact resistivity and not give significant contribution to device defectivity.

In previous study,[2] it was reported that the TiN/$TiSi_2$ structure is formed during thermal annealing of TiN_X film. The overlying TiN was relatively thick and the $TiSi_2$ is rather thin and uniform. In this report, we will describe the successful utilization of the TiN_X as a diffusion barrier for the W bit-line in COB structured DRAM fabrication process.

2. EXPERIMENT

The (100) p-type silicon wafer, with 10-20 Ω · cm resistivity, was used as the substrate. In order to evaluate the barrier property of TiN_X, following samples were prepared. After deposition of 500 nm thick CVD oxide, bit contacts of 0.4 μm in diameter were defined using conventional reactive ion etch (RIE) technique. TiN_X film of 50 nm thickness was deposited using conventional reactive sputtering at the mixed atmosphere of Ar and N_2, in which the N_2 volume percent was fixed at 15. Thermal annealing was carried out at temperature ranges of 600~700℃, which results in the formation of TiN/$TiSi_2$ bilayer. CVD W of 200 nm thickness was deposited and followed by the delineation using RIE. After deposition of passivation oxide of 500 nm thickness, the samples were annealed at the temperature of 600~870℃ for 9 hours. For comparison of TiN_X's barrier properties with conventional TiN (con-TiN), the samples were fabricated with the same procedure except the formation of diffusion barrier layer, that is, con-TiN/Ti. To evaluate the electrical properties of the W/TiN_X bit-line, full processes needed in DRAM, as summarized in Table 1, were performed. And this results were compared with those of the polycide. The samples were analyzed using SEM, TEM, FIB, and electrical parameter analyzers.

3. Results and Discussion

The composition of as-deposited TiN_X film is identified to be $TiN_{0.6}$, according to RBS analysis, and the film is composed of nanocrystalline structure consisting of Ti and TiN.[2] Therefore, it is easily conjectured that the structure of TiN, formed during thermal annealing, would be more stabilized compared with the conventional TiN, which shows a columnar structured grain-boundary.

Figure 1 shows the cross-sectional image of the sample which used the TiN_X as the barrier after thermal annealing at 870℃ for 9 hours. It should be pointed out that two-step thermal annealing preocess (600℃, 30sec and 700℃ for 30sec) was carried out for the formation of TiN/$TiSi_2$ bilayer. It is also worthwhile to note that it it was found that not only the formed TiN bears out severe thermal budget, but also a thin $TiSi_2$ layer forms below the TiN even after the thermal

annealing. Moreover, any defects were found in TEM study.

In constrast with the TiN_X case, however, the sample which adopted the conventional TiN as a barrier layer exhibits the excessive formation of WSi_2 due to the destruction of the barrier layer, as shown in Fig. 2. Severe defects, such as void [Fig. 2(a)] and wormhole [Fig. 2(b)], are observed. The former is due to the diffusion of Si atoms from the substrate through the excessively formed WSi_2.[1] Specifically, the latter, which is reported as a general defect generated in selective tungsten deposition process,[3] suggests that WF_X or F atoms diffuse through grain boundary of the conventional TiN toward the Si substrate. It should be noted that the above W deposition process was performed under hydrogen reduction process.

The line resistance of the polycide and the W/TiN_X bit-line after thermal annealing at the temperature ranges of 600-870℃ is shown in Fig. 3. The resistance of the W/TiN_X bit-line (less than 1.2 Ω/□) is two order-of-magnitude lower than that of the polycide bit-line (higher than 130 Ω/□). This is due to the lower resistivity of W (about 10 μΩ · cm),[4] which suggests the feasibility of W as a bit-line in COB structured DRAM.

The contact resistance of the bit-lines' contact resistance depending on annealing temperature is shown in Fig. 4. Although the contact resistance of the polycide, measured by 420 contact chains of the same samples shown in Fig. 3, abruptly decreases after thermal annealing above 700℃ due to the activation of CVD WSi_2, the value shows still higher value than the W/TiN_X's. While the value of the W/TiN_X contacted bit junctions shows nearly constant (about 100 Ω/contact) irrespective of annealing temperature.

Figure 5 shows the contact resistance variation of the bit-line contact as a function of contact size, which was fabricated by the procedure shown in Table 1. The resistance of the W/TiN_X contacted bit-junction shows two-thirds as low as that of the polycide, as predicted in Fig, 4. Figure 6 show the leakage current distribution of n^- and n^+ bit-junction, which was measured at reversed vias voltage of 6. The mean value and the uniformity of the W/TiN_X bit-junction are lower and sharper than those of the polycide bit-junction. Considering that the electrical properties, such as contact resistance and leakage current, are related with the thickness of $TiSi_2$ and the barrier property of TiN,[5] such a behaviour of the TiN_X conatcted bit-junction could be explained by the formation of stable $TiSi_2$ layer under the TiN and stability of the TiN.

4. CONCLUSION

The TiN_X as a diffusion barrier for the application of W bit-line in COB DRAM and its feasibilities was described. It was found that the TiN_X layer sufficiently bears out the severe thermal budget applied in the fabrication process. Also, the electrical properties of the W/TiN_X bit-line are superior to those of polycide bit-line.

Reference

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● Isolation and Junction formation ● CVD oxide (5000Å) deposition ● Bit contact (0.4μm in diameter) etch
⬇
● TiN_X deposition (500Å) ● 2-step RTA at 600-700℃
⬇
● CVD W (2000Å) deposition ● Bit line delineation (0.4μm in width)
⬇
● Capacitor formation (~800℃) ● BPSG flowing (~870℃) ● Contact and Al metallization
⬇
● Evaluation : Structure : SEM, TEM Electical Property : leakage current and contact resistance

Table 1. Process sequence

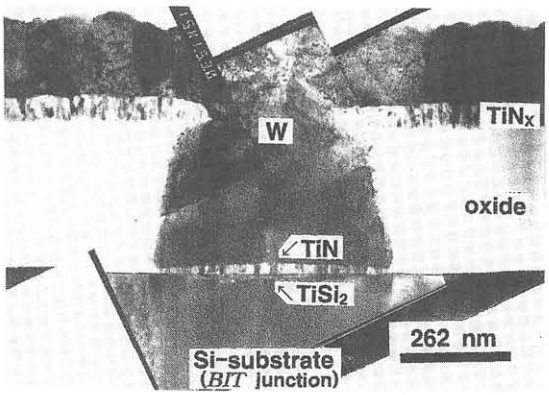

Fig. 1. XTEM image of the sample showing the formation of TiN/$TiSi_2$ and its barrier property against W after annealing at 870℃ for 9 hours.

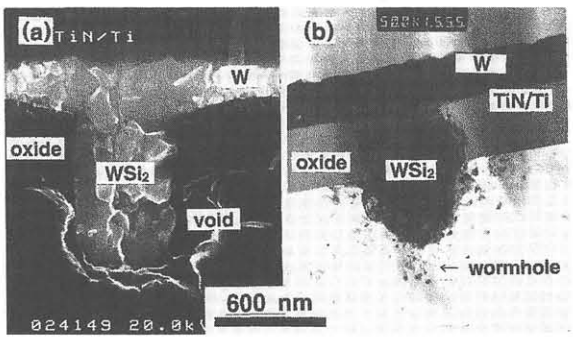

Fig. 2. (a) SEM and (b) XTEM image of the sample using conventional TiN as W barrier after annealing at 870℃ for 9 hours.

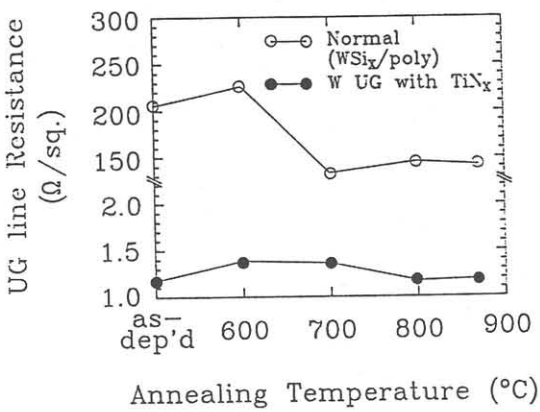

Fig. 3. Bit line resistance of the polycide and the W/TiN_X as a function of annealing temperature.

Fig. 6. Leakage current of (a) n^- and (b) n^+ bit-junction. The bit line (or contact) was formed by the polycide and the W/TiN_X. (right)

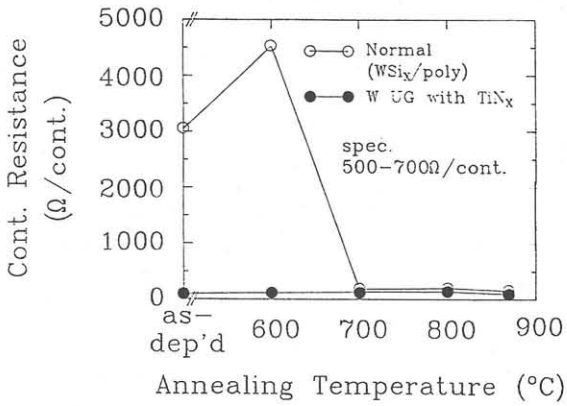

Fig. 4. Contact resistance of the polycide and the W/TiN_X contacted bit junction as a function of thermal annealing temperature.

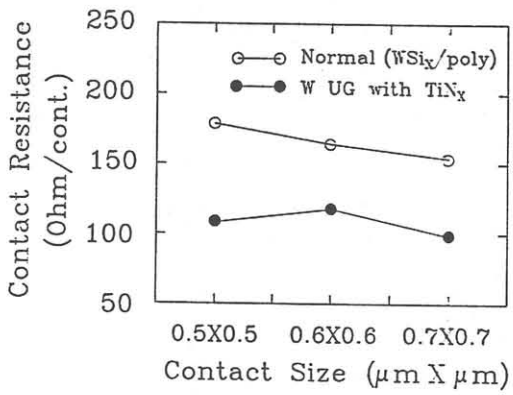

Fig. 5. Contact resistance of COB DRAM's bit junction as a function of contact size. The bit line (or contact) was formed by the polycide and the W/TiN_X.