Extended Abstracts of the 1995 International Conference on Solid State Devices and Materials, Osaka, 1995, pp. 82-84 S-IV-5

Invited

Formation of Metal/Silicon Contacts for ULSI and Induced Defects by Silicidation

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We have investigated crystallographic structures and electrical properties at the interfaces of transition metals such as Ti, Zr, Hf and V and Si(100), from the viewpoint of an application to ohmic contacts in future ULSI's with low contact resistivity and high reliability. The silicidation reaction at 400-600°C brings about the formation of deep levels associated with vacancies or with metal atoms, related to the silicide formation process. Furthermore, an anomalous electrical characteristic observed for Hf/p-Si contacts is markedly improved by a H-termination treatment of Si surfaces.

1. INTRODUCTION

Formation of ohmic contacts with low contact resistance and high reliability is one of the key issues in realizing future ultra-large scale integrated circuits (ULSI's). Transition metals in the group IVa, Va and VIa and their silicides can be expected to be low-resistivity contact materials for ULSI's. We have investigated crystallographic structures and electrical characteristics of the interfaces between these metals and Si(100) substrates and reported contact resistivities of 3-5x10^{-8} Ωcm^2 in Zr/ and Hf/n$^+$-Si(100) at annealing temperatures of 400-600°C,[1-3] which is summarized in Table I.[4]

The silicidation reaction at the interface also induces the formation of defects such as vacancies and diffused metal atoms. These defects are thought to cause the increase in leakage current and to impede the precise control of impurity profiles of very shallow pn junctions. Therefore, understanding interfacial phenomena related to solid-phase reactions are necessary in order to form highly-reliable ohmic contacts.

In the present study, we have examined the formation of interfacial defects by the silicidation reaction and the effect of H-termination of Si(100) surfaces on the electrical properties. The H-termination of Si surfaces is promising as a new technology for surface passivation to control the formation of native oxide. A marked improvement of the electrical characteristics in p-Si Schottky diodes has been found upon H-termination treatments.[5]

2. EXPERIMENTAL

Substrates used were n- and p-type Si(100) wafers with a resistivity of 0.5-0.7 and 1-3 Ωcm, respectively. Si wafers were chemically cleaned and dipped in a diluted HF solution (HF:H_2O=1:50) to remove thin oxide layers and rinsed in deionized (DI) water for 10 min before placing in an ultrahigh-vacuum (UHV) evaporation chamber with a base pressure less than 5x10^{-10} Torr. After introducing the substrates into the UHV chamber, transition metal films were deposited using an electron-beam evaporator and then the samples were thermally annealed at 400-600°C for 30 min in the chamber.

In order to examine electrical properties of metal/Si interfaces, Schottky diodes were formed on the Si(100) substrates. Schottky barrier heights were determined from the temperature dependence of I-V characteristics and also capacitance-voltage (C-V) characteristics at 1 MHz. Furthermore, deep levels at the metal/Si interface were examined by deep-level transient spectroscopy (DLTS).

3. RESULTS AND DISCUSSION

3.1 *Formation of defects*

Figure 1 shows DLTS spectra of Hf/n-Si(100) diodes at various annealing temperatures.[6] We can observe several peaks in the DLTS spectrum for the as-deposited sample, and it should be noted that these peak intensities are drastically reduced by annealing. After annealing at 460 and 580°C, a bilayer structure consisting of an amorphous layer and an epitaxially-grown layer of Hf_3Si_2 is formed between Hf films and Si(100) substrates.[3] Therefore, it can be considered that the growth of epitaxial Hf_3Si_2 layers leads to a decrease in trap densities. The minimum values of ρ_c are obtained at 580°C in this system.

The energy levels of electron traps denoted by E1, E2 and E4 in Fig. 2 are determined by Arrhenius plots as E_c-E_t=0.15±0.01, 0.20±0.05 and 0.43±0.03 eV, respectively. The trap E1 can be assigned to a complex of Si vacancies and O atoms (0.17 eV),[7] which is not observed for samples with H-termination. The trap energies of E2 and E4 are very close to those of divacancies (0.23 and 0.43 eV)[7-9] and a complex of vacancies and P atoms (0.44 eV).[7, 9] The average trap densities of E1, E2, and E4 are about 2x10^{13}, 3x10^{12} and 1x10^{14} cm^{-3}, respectively. The densities of these vacancy-related traps are reduced by annealing, e. g., the values of E1, E2 and E4 for the sample annealed at 460°C are 1/3-1/10 times smaller than those for as-deposited one. After annealing at 580°C, these vacancy-related traps are vanished, which means that the densities are less than 10^{11} cm^{-3}. The DLTS signals of E3 (0.29±0.01 eV) and E5 at 460°C, the origins of which are not clear yet, were less than the detection limit of DLTS measurements. A new

Table I. Minimum contact resistivities and the corresponding annealing temperatures for Ti, Zr, Hf, V and Cr/n$^+$- and p$^+$-Si(100) contacts.[4] P and B concentrations in n$^+$- and p$^+$-Si diffused layers in the Kelvin patterns were 2x10^{20} and 1x10^{20} cm^{-3}, respectively.

Metal	ρ_{cn} (Ωcm^2)	Annealing Temp. (°C)	ρ_{cp} (Ωcm^2)	Annealing Temp. (°C)
Ti	2.4x10^{-7}	520	2.8x10^{-7}	580
Zr	3.4x10^{-8}	420	1.8x10^{-7}	560
Hf	5.4x10^{-8}	580	1.8x10^{-7}	560
V	1.3x10^{-7}	550	2.1x10^{-7}	550
Cr	2.2x10^{-7}	350	2.1x10^{-7} (<2x10^{-8}	450 as-grown)

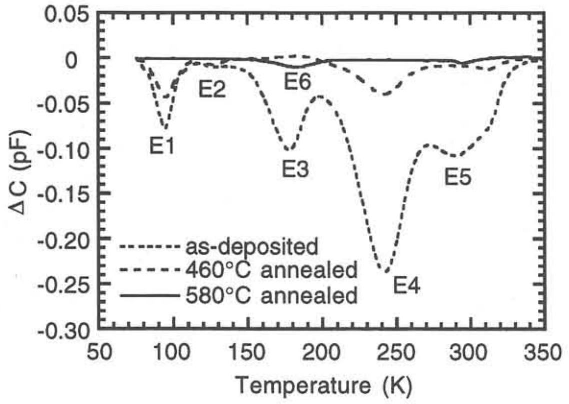

Fig. 1. DLTS spectra of Hf/n-Si(100) with various annealing temperatures.

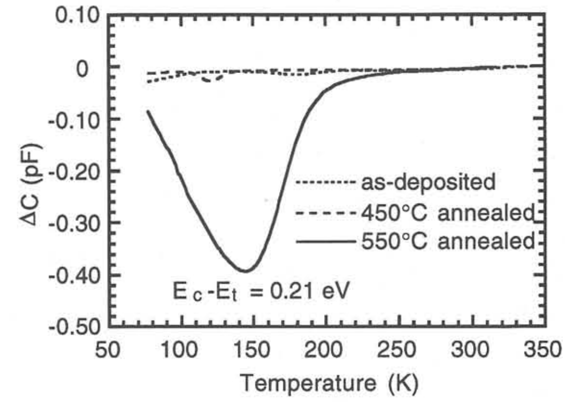

Fig. 2. DLTS spectra of V/n-Si(100) with various annealing temperatures.

trap, labeled E6, is produced at 580°C, which has an activation energy and an average density of 0.29±0.02 eV and $1x10^{12}$ cm^{-3}, respectively. The formation of vacancy-related traps observed in Fig. 1 is related with the interfacial reaction, as discussed below.

In the case of V/n-Si diodes, however, we do not observe any vacancy-related traps. Figure 2 shows the DLTS spectra of V/n-Si(100) at various annealing temperatures.[10] In the as-grown sample, DLTS signals are very small. By annealing up to 550°C we can observe a marked increase in DLTS signals with increasing annealing temperature. In this temperature range, the energy level of an electron trap is determined to be E_c-E_t=0.21±0.02 eV, the concentration of which is about $8x10^{12}$ and $4x10^{14}$ cm^{-3} at 450 and 550°C, respectively. Vanadium atoms are reported to be fast diffusers in Si substrates[11] and this trap can be identical with an acceptor level of interstitial vanadium atoms.[12] The metal atom diffusion into Si substrates is also observed for Ti/Si systems in this temperature range.[13]

The formation of different types of traps between Hf and V by annealing is considered to be closely connected with silicidation reaction at the interface. The silicidation reaction at the Hf/Si interface has been reported to be limited by diffusion of Si atoms in silicide layers.[14] In addition, the interfacial reaction is initiated by the existence of SiO_2 on Si surfaces and the silicidation takes place even for as-deposited samples.[3, 15] Therefore, the vacancy-related traps observed in Hf/Si are thought to be formed as a result of the silicidation reaction. Vacancy-related traps are also detected for Hf/p-Si, as shown in Fig. 4. In the case of V/Si(100) systems, on the other hand, the density of traps related with interstitial V atoms is markedly increased with an increase in annealing temperature. It has been reported that the diffusion of V atoms into the Si substrate is dominated in the silicidation process below 650°C.[10] Furthermore, the relatively good Schottky characteristics can be obtained and the n-values are also close to unity for both V/n- and V/p-Si.[10] These facts suggest that the silicide formation process also dominates the electrical characteristics at metal/Si interfaces.

3.2 *H-termination effects on electrical characteristics*

The termination of dangling bonds with H atoms makes Si surfaces passive against oxygen adsorption even in atmosphere.[16] H-terminated Si(100) surfaces can be obtained by dipping in a HF solution and then rinsing in DI water for a very short time.[17, 18] In this experiment, Si substrates were rinsed in DI water for 2-5 s to obtain H-terminated Si(100) surfaces and the H-termination was confirmed by high-resolution electron energy loss spectroscopy (HREELS) and x-ray photoelectron spectroscopy (XPS) measurements. Figures 3(a) and 3(b) show the forward I-V characteristics of as-deposited Hf/p-Si(100) diodes formed on the nonterminated and the H-terminated surface, respectively.[5] In Fig. 3, the n-values obtained from the linear part in log$I$ versus V plots are also listed. In the case of nonterminated diodes, the n-value deviates significantly from unity and the I-V characteristics are far from the ideal thermionic emission characteristic, which is considered to be affected by the interfacial oxide. On the other hand, the current is found to be dominated by the thermionic emission and the n-value of H-terminated diodes is very close to unity. The results in Fig. 3 clearly show that the I-V characteristics of Hf/p-Si diodes are markedly improved by the H-termination of Si surfaces even for as-deposited diodes. The reverse I-V characteristics are also improved by H-termination.[5]

The characteristic features of nonterminated p-Si diodes are that the n-values are much larger than unity and, moreover, that anomalous large barrier heights are obtained from C-V characteristics.[2] A possible explanation for the anomaly observed in nonterminated diodes is the formation of a dielectric-like layer at the interface,[2, 19] which is considered to act as a series capacitance in C-V characteristics. Since the H-termination protects Si surfaces from native oxidation and adsorption of O atoms, the main reason of the anomalous characteristics observed at nonterminated p-Si interfaces is thought to be related with native oxide. However, the anomaly is observed even after annealing at 580°C. Since the native oxide layer of Si is reduced by Hf,[3] the dielectric-like layer is considered to be formed as a result of the solid-phase reaction.

Measured DLTS spectra of H-terminated Hf/p-Si(100) diodes are shown in Fig. 4.[5] For nonterminated p-Si diodes, DLTS spectra could not be measured because of very large reverse current. For as-deposited diodes with H-termination, the DLTS peaks of both electron and hole traps can be observed. Unfortunately, the trap energies cannot be determined, because of an overlap of these peaks. After the annealing at 460°C, three kinds of hole

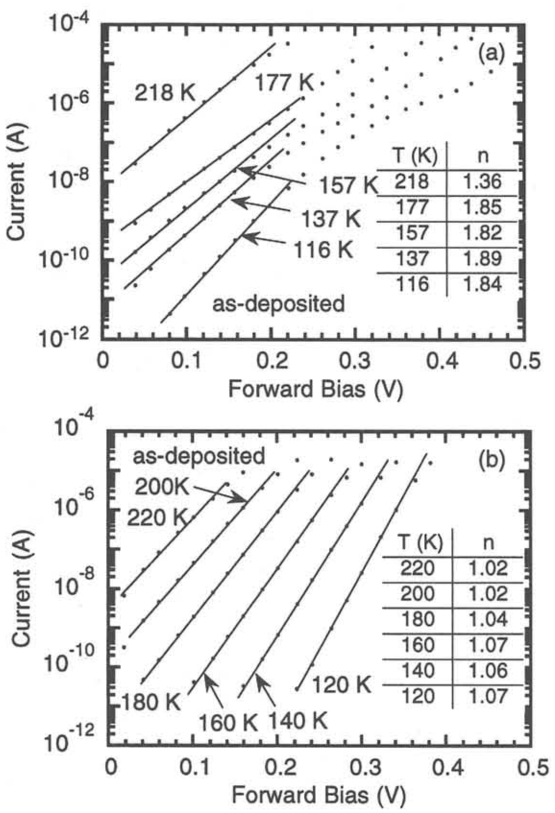

Fig. 3. Forward current-voltage characteristics of as-deposited Hf/p-Si(100) formed on (a) nonterminated and (b) H-terminated Si surfaces.

traps denoted by H1, H2 and H3 are produced, the energy levels of which are E_t-E_v=0.14±0.01, 0.43±0.02 and 0.52±0.02 eV, respectively. The origin of H1 is considered to be due to Si vacancies (0.13 eV)[20] and those of H2 and H3 are complexes of B atoms with vacancies or interstitial Si atoms,[21] whose average densities are 4×10^{12}, 1×10^{13} and 1×10^{13} cm^{-3}, respectively. These vacancy/interstitial-related traps are considered to be formed by the silicidation at 460°C. These traps are annealed out and only a small electron trap signal can be observed by annealing at 580°C.

4. Conclusions

We have investigated the defect formation by silicidation reaction and the H-termination effect on electrical characteristics of transition-metal/Si(100) interfaces. It is found that the silicidation reaction at annealing temperatures of 400-600°C yields vacancy/interstitial-related traps at the Hf/Si interface and interstitial metal atom-related traps at V/Si. The silicide formation process is considered to have a close connection with the production of these traps.

The H-terminated Si(100) surface is confirmed to be very stable for the formation of native oxide and the adsorption of oxygen. From I-V and C-V measurements, it can be concluded that the electrical characteristics of Hf/p-Si diodes are markedly improved by the H-termination. It is also found that the H-terminated Hf/p-Si interface has a very low density of defects. Therefore, we can conclude that the H-termination of Si surfaces is very effective in controlling and improving the metal/p-Si interfacial properties.

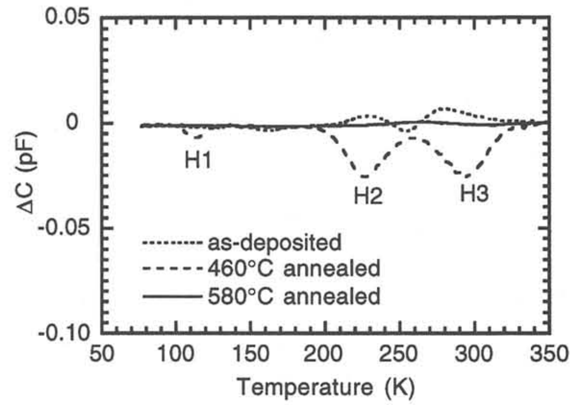

Fig. 4. DLTS spectra for as-deposited, 460°C-annealed and 580°C-annealed Hf/p-Si(100) diodes with H-termination.

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