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Invited

Atomic-Scale and Hierarchical Modeling for Nano-Electronics

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Nano-electronics process and device modeling pose new challenges to traditional technology CAD in view of abstraction of functional behavior in a complex system, where model hierarchy needs to be established to tackle the computational complexity. In view of predictive accuracy during technology advancement, atomic-scale modeling is now necessary for more invariant physical effects. Critical issues on the atomic-scale and hierarchical modeling will be discussed in various technology directions.

1 Introduction

The ongoing scaling of IC technology will result in MOS devices with gate lengths below 1000A by the turn of the century; prototype devices have already been demonstrated. For storage technologies such as dRAM and Flash EEPROM, fundamental dielectric and other reliability limitations pose major roadblocks to further scaling. Research into alternative materials, single electron and quantum phenomena are all receiving increased attention. Finally, interconnection scaling has now replaced intrinsic device effects as the dominant industrial concern, impacting clock speeds and signal integrity---especially for mixed-signal systems. This talk focuses on the needs and new modeling opportunities across a hierarchy of technology and systems issues.

2 Model Hierarchy

Over the past two decades technology computer-aided design (TCAD) has become well-established and broadly used in support of process, device and circuit modeling of IC technology. Support for SPICE models at the circuit level through underlying device/interconnect design at the technology level can now be achieved using highly integrated, user-friendly TCAD workbenches that include first-generation "virtual fab" capabilities. For example, predictive threshold voltage scaling, including reverse short channel and subthreshold effects, are achieved based on accurate 2D process and device simulations [1]. Presently TCAD also provides valuable information on geometrically distributive parasitic effects for analog design and manufacturing variations for yield analyses. Nonetheless, the rate of technology scaling now faces fundamental and atomic-scale limits where new modeling approaches will be required. Figure 1 shows the dimension and time scales involved in moving from equipment and continuum process modeling (used for current TCAD tools) into the mesoscopic, quantum molecular and atomic scale modeling regimes. The issues of hierarchical feed-forward encapsulation of data used at higher levels is an important issue to be considered.

3 Atomic Scale Microscopic Modeling

The evidence concerning the needs for atomic scale microscopic modeling are clearly reflected in both device- and process-level effects observed in emerging technologies; examples help to illustrate these trends. Figure 2 shows the schematic cross-section of a proposed hot electron structure in silicon (HESS) device, including Monte Carlo results of carrier distributions at the collector surface [2]. The possibilities for such structures as sub-picosecond switching devices and potential replacements of conventional Flash EEPROM technology depend critically on quantifying advanced carrier transport effects in conjunction with realizing technologically viable structures. A second modeling example comes from the process technology domain and considers the fundamental issues required to support fabrication of single-electron devices [3]. In the case of charge storage (and Coulomb blockage) in atomic-scale silicon islands imbedded in thin dielectrics formed by aggressive oxidation [3] or nucleation [4] with typical size of about 40 nm, the fundamental understanding of process control for these islands will be critical. Figure 3 shows results of molecular dynamic simulations of nucleation and growth of such islands starting from deposited amorphous silicon layers [4]. These results suggest that perfect spherical silicon crystals with uniform size and spacing can be grown. Electrical connection to these islands are currently under development. Through the atomic-level simulation results and methodology it is possible to more quantitatively evaluate the process control and material dependences of such atomic-scale device technologies.

4 Hierarchical Extraction Methodology

As indicated by the above examples, there are very promising and challenging devices and technology opportunities that can exploit atomic-scale effects and benefit from emerging simulation capabilities at these levels. Yet in order to exploit these phenomena the information must be made available at higher levels. Extraction of SPICE-level parameters directly from

quantum calculations has been demonstrated in EEPROM modeling [5]. The following examples illustrate progress in hierarchical extraction through macroscopic process and device levels. Figure 4 shows schematically the connection of tools and the hierarchical imbedding of material coefficients (Cii & Cij) required for the stress-dependent simulation of local oxidation using continuum models. The functional forms and parameters for both process simulation (TSUPREM) and stress simulation (ABAQUS) based on continuum (partial differential equation) representations are supported using molecular dynamic and even ab-initio simulations [6,7]. The predictive extraction of these coefficients is an essential part of helping to deconvolve both fundamental questions about the physics and metrology of complex isolation structures with thin dielectric layers [8].

Due to the nonlinear scattering rates and full band effects, it is difficult to characterize continuum hot carrier models for generalized applications directly from measurements. However, device operations such as the HESS transistors [2] and device reliability analyses such as the substrate and gate current of MOSFETs critically depend on accurate hot carrier models. Device Monte Carlo simulation suffers from statistical noise and high computational cost. The two-population continuum hot carrier model [9] is further improved to use only the parameters fed forward from bulk Monte Carlo simulation through integration of the distribution function and scattering rates.

5 Higher-level Behavioral Models

It is essential that higher-level behavior must be extracted. Progress in interconnect technology and modeling is a rate-limiting factor in VLSI as well as radio frequency (RF), mixed-signal systems. Figure 5 shows both a "virtual wafer" model of cell-level interconnects for an sRAM along with supporting simulation requirements for modeling: metal/grain-boundary effects, step-coverage of inter-layer dielectric deposition/etching and substrate stress effects due to local oxidation. The complexity of these interconnect structures pose a major challenge in designing for manufacturability (DFM) and in extraction of physically correct behavior models. Due to the use of multi-layers the interactions of structural and behavioral effects are closely linked. TCAD-based reference standards for local interconnect libraries have been demonstrated and are becoming of system-level importance in support of ERC and signal integrity verification [10]. Such models can predictively track technology dependences and trends as reflected in Figure 5.

The importance of RF behavior in mixed-signal systems pushes the modeling boundaries of both devices and the interconnect. The harmonic-balance (HB) technique is broadly used in the RF community for analyzing signal distortion and intermodulation (IM). We have recently demonstrated a device-level simulator (PISCES-HB) that exploits this analysis methodology and supports the extraction of higher-level behavior models [11]. From a hierarchical point of view, this allows the direct extraction of compact models using PISCES-HB as part of a "virtual spectrum analyzer". At a physical level, it is now possible to explore optimization of technology to minimize distortion using the detailed information inside the structure.

6 Conclusion

To meet the future challenges of complex system design in IC technologies, hierarchical models ranging from atomic to behavior levels are invaluable for performance/yield optimization and time-to-market minimization. With some preliminary results shown in the previous sections, research on atomic-level modeling and abstraction methodology in model hierarchy will become increasingly important.

7 Acknowledgments

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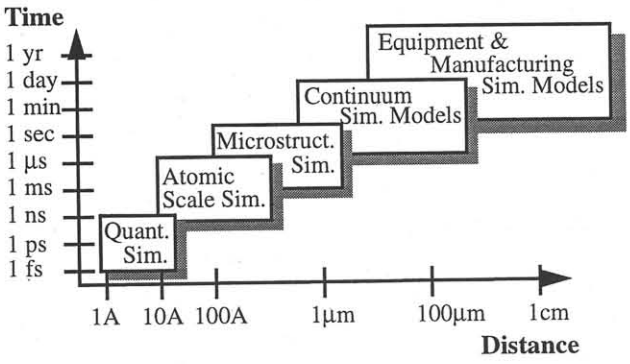

Fig1: Dimension and time scales in TCAD modeling.

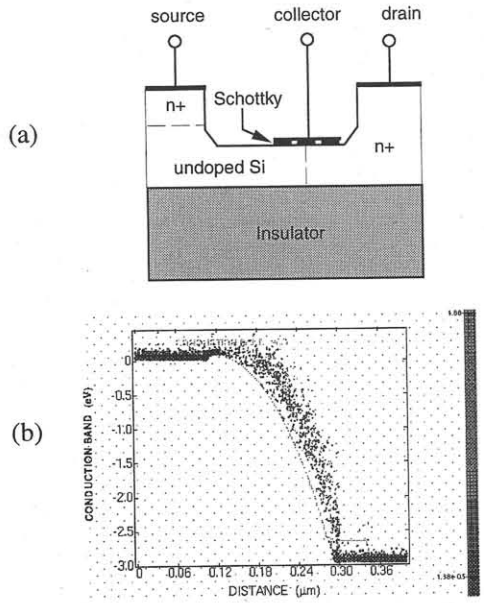

Fig. 2: A novel hot electron structure in silicon (HESS) device: (a) the schematic cross-section; (b) Monte Carlo results of carrier distributions at the collector surface.

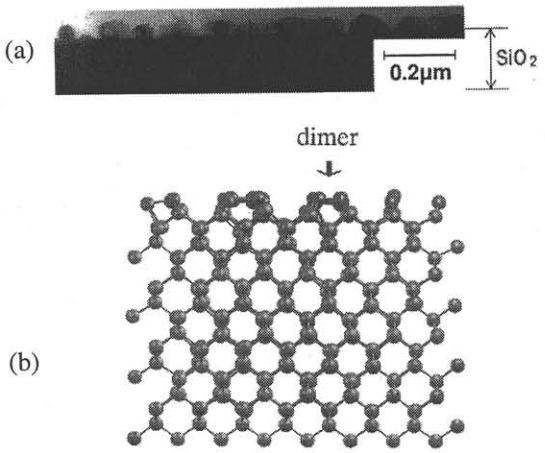

Fig. 3: Nucleation of silicon islands from deposited amorphous silicon substrate: (a) TEM image; (b) molecular dynamic simulation.

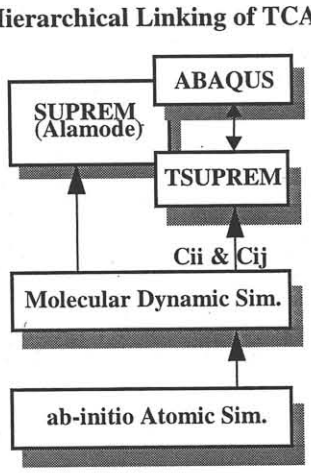

Fig. 4: Connection of tools in the hierarchical modeling of material coefficients Cii and Cij.

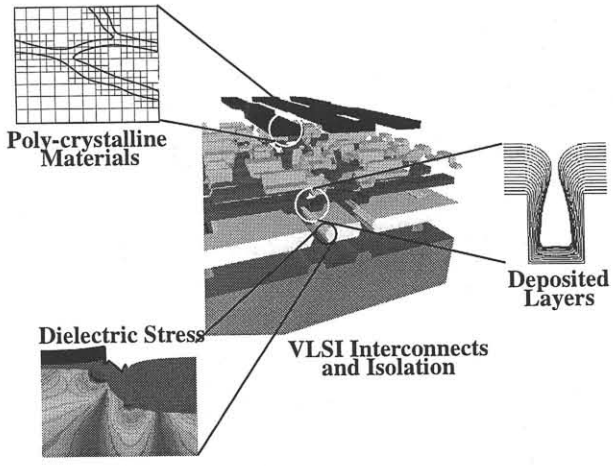

Fig. 5: A virtual-wafer model of cell-level interconnects for an SRAM cell.