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New Method of Extracting Inversion Layer Thickness and Charge Profile and Its Impact on Scaled MOSFETs

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We have developed a new method of extracting the inversion layer thickness and carrier profile using gate-channel capacitance measurements. The experimental results of our method showed good agreement with published quantum mechanical calculations. We have applied this method to both bulk and SOI MOSFETs including double-gated devices and demonstrated that we can investigate carrier behavior inside the highly scaled MOSFETs using this method.

1. Introduction

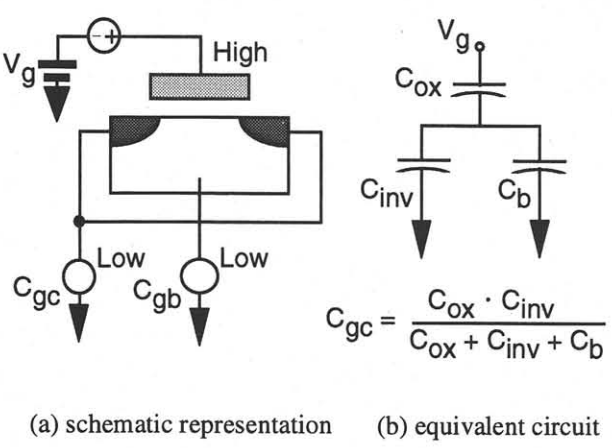
As MOSFET technology is extended into the tenth-micron range and the gate oxide thickness is scaled to less than 5 nm, the device transconductance degradation becomes a severe problem. This problem is due to effects from the non-negligible inversion layer thickness and its finite capacitance, which is in series with the gate-oxide capacitance [1]. It is important to extract the carrier profile in the inversion layer to understand its effect on device performance. So far there have only been quantum mechanical calculations, but no experimental method to characterize the inversion charge profile.

2. New extraction method

In order to extract the inversion layer thickness and carrier profiles experimentally, we used two sets of data. One is the dependence of the inversion charge, Q_{inv}, on gate voltage. Where Q_{inv} is obtained from the integration of the gate-channel capacitance, C_{gc}. The other is the dependence of the average location of the *incremental inversion charge*, $X_{increment}$, on gate voltage. Where $X_{increment}$ is the average increment of the inversion charge thickness, in accordance with a small gate voltage change. This thickness can be defined as

$$X_{increment} = \varepsilon_{Si} / C_{inv}, \qquad (1)$$

where ε_{Si} is the permitivity of silicon and C_{inv} is the inversion layer capacitance. Both sets of data can be obtained from the conventional split C-V measurements shown in Figure 1. Figure 2 shows a schematic representation of our method. Each triangular segment



(a) schematic representation (b) equivalent circuit

Fig. 1. Split C-V measurement.

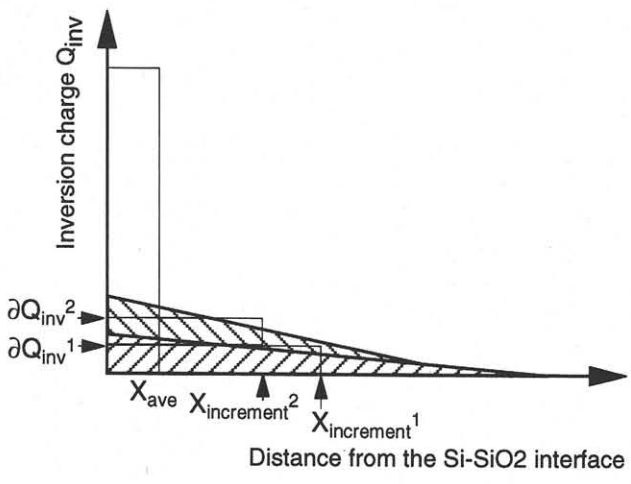


Fig. 2. Schematic representation of extraction method.

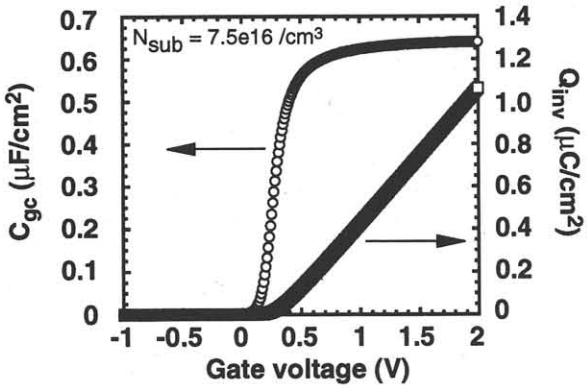


Fig. 3. Dependence of C_{gc} and Q_{inv} on gate voltage. The device is a single-gated SOI nMOSFET with a 5.4-nm-thick gate oxide and a 40-nm-thick Si layer.

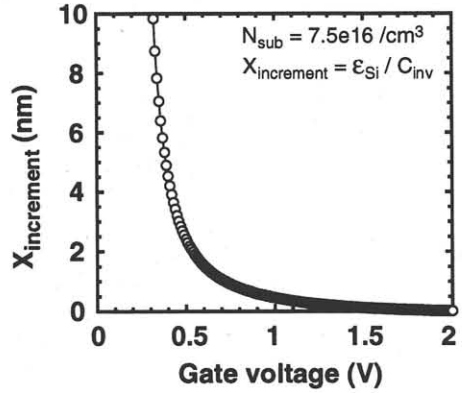


Fig. 4. Dependence of $X_{increment}$ on gate voltage. $X_{increment}$ represents the average location of the incremental inversion charge in accordance with the small change of gate voltage.

represents the actual distribution of the incremental inversion charge, $\partial Q_{inv}{}^{i}$, in accordance with a small change in gate voltage. We can assume that the incremental inversion charge exists within $X_{increment}{}^{i}$. Therefore, we can obtain the average thickness of the inversion layer, X_{ave}, using the expression

$$X_{ave} = \int_{V_{FB}}^{V_g} C_{gc}(V_g) X_{increment}(V_g) dV_g \Big/ \int_{V_{FB}}^{V_g} C_{gc} d V_g, \quad (2)$$

where V_{FB} is the flat-band voltage. We can also obtain the inversion charge profile by plotting two sets of data, as in Figure 2. We applied this method to a single-gated SOI nMOSFET with a 5.4-nm-thick gate oxide and a 40-nm-thick Si layer. Figure 3 shows the experimental result for the gate-channel capacitance, C_{gc}, and its integration, Q_{inv}. Figure 4 shows the gate voltage dependence of $X_{increment}$. Our results and Baccarani's quantum mechanical calculation results [2] for the inversion layer thickness are shown in Figure 5. The experimental results are quite close to the quantum mechanical calculation. The inversion charge behavior can be obtained experimentally with our new method.

3. Impact on Scaled MOSFETs

In order to investigate the effect of gate oxide scaling on current drivability, we applied our experimental method to bulk MOSFETs with various gate oxide thicknesses. Figure 6 shows the ratio of the inversion layer

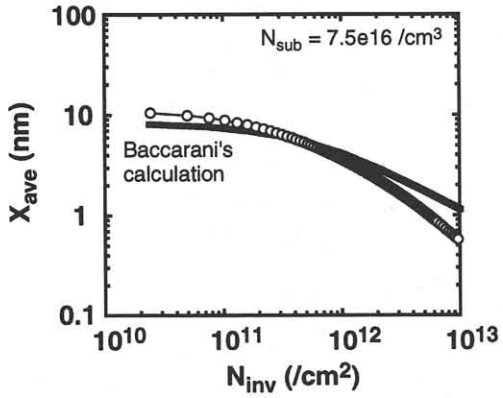


Fig. 5. Dependence of inversion layer thickness on inversion charge density. X_{ave} is calculated using two sets of data from Figs. 3 and 4. The device is a single-gated SOI nMOSFET.

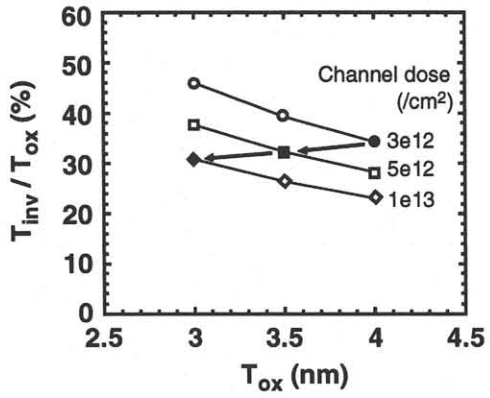


Fig. 6. Ratio of inversion layer thickness to gate oxide thickness. All the devices are bulk nMOSFETs with gate oxides of less than 4 nm. T_{inv} is equal to X_{ave}.

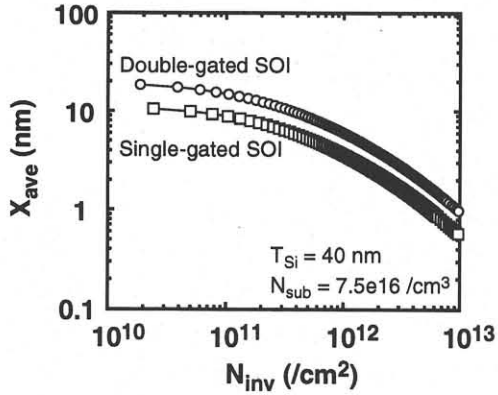


Fig. 7. Comparison of inversion layer thickness.
The double-gated SOI MOSFET has an additional back-gate electrode in the buried oxide layer. The back-gate electrode is connected with the front-gate electrode.

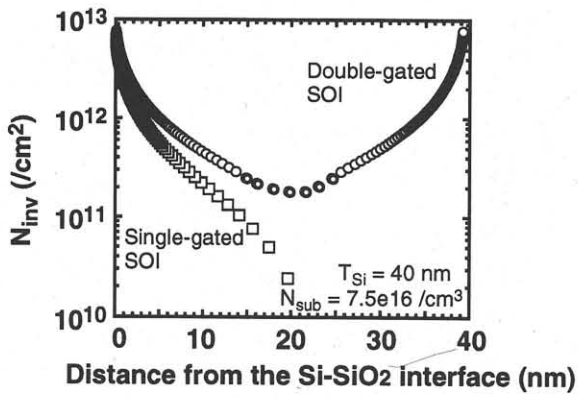


Fig. 8. Inversion charge profile in the Si layer.
The double-gated SOI MOSFET has an inversion charge of more than 1e11/cm^2, even at the center of the Si layer.

thickness to the gate oxide thickness for bulk nMOSFETs. The ratio increased with decreased gate oxide thickness, thus causing transconductance degradation, due to the non-negligible inversion layer thickness effects. However, gate oxide scaling is accompanied by an increase in the channel impurity concentration to suppress short-channel effects. This means the ratio does not increase, as indicated by the arrows in Figure 6, so that the current drivability does not degrade for scaled MOSFETs with a gate oxide less than 4 nm. We also applied our method to both single- and double-gated SOI MOSFETs, which is considered one of the most promising future devices [3]. Figure 7 shows a comparison of the inversion layer thickness. The double-gated SOI MOSFET has a thick inversion layer, compared with the single-gated SOI MOSFET. This is consistent with a reduced normal surface electric field and the resultant high carrier mobility in double-gated SOI MOSFETs. Figure 8 shows inversion charge profiles in the Si layer for both single- and double-gated SOI MOSFETs at a gate voltage of 2 V. Note that the double-gated SOI MOSFET has an inversion charge of more than 1e11 cm-2, even at the center of the Si layer. To our knowledge, this is the first time that the inversion charge profile has been obtained and the volume inversion phenomena observed experimentally.

4. Conclusion

We developed a new method to extract the inversion layer thickness and carrier profile using gate-channel capacitance measurements. Our results shows good agreement with published quantum mechanical calculations. We have applied this method to both bulk and SOI MOSFETs, including double-gated SOI devices. This method can be used to investigate the carrier behavior of scaled MOSFETs.

Acknowledgment

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