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An Approach for Migrating to Low Voltage and Low Power ULSIs

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1. INTRODUCTION

Current ULSI micro-fabrication technologies are still being pushed to new extremes by the DRAM community, thereby expediting research on 1 - 4 Giga-bit DRAMs[1] using 0.16 - 0.1 μm design rules. The giga-scale integration (GSI) era has already begun. Also, sophisticated microprocessors using 0.2-0.1 μm MOSFETs could possibly appear at the beginning of the 21st century. Combined with such finer-line technologies, much diversified LSI application to multi-medias, personal digital assistants (PDA) and information appliances is now opening the "nomadic computing" age, which will bring about the paradigm shift to our life and society. Key technologies underlying this trend are low power, low cost, high performance, and high reliability. Additionally, new approaches to ULSI systems and architectures have been proposed to enhance the total performance of systems and to reduce system cost. Examples include the embedded DRAMs[2] that overcome bandwidth bottlenecks, network-centric computing systems independent of OS/machines, and audio-video computing systems (MPEG).

For scaled MOSFETs, thin film SOI devices will be most promising for low power as well as short channel effects in spite that a crystal quality problem still remains. However, along with the drastic paradigm shift occurring in semiconductor business and technology, a new strategy, in particular for low power electronics must be introduced to realize the nomadic lifestyle armed with the easy-to-use giga chips. In this paper, state-of-the-art ULSI technology is reviewed and the new challenges for giga-scale integration (GSI) from the view points of low power and low voltage are presented.

2. DRAM TECHNOLOGY

DRAMs are now suffering from process complexity due to the complicated 3-D cell structures needed to reduce soft error rate, leading to increased bit-cost and a speed gap between MPUs and memories. The former strongly requires use of ferroelectric materials such as PZTs in the memory capacitor; the latter requires embedded DRAMs aiming at more system-oriented applications. The embedded memories provide low power consumption due to smaller load capacitance within a chip as well as enhanced band width.

2.1 Ferroelectric DRAM

The solution to complicated three-dimensional cell structures is use of ferroelectric materials such as PZT as capacitor insulator. By using PZT as the ferroelectric material, as well as high-dielectric material, a new nonvolatile low power memory[3] is created, which operates as a conventional DRAM in the power-on mode and as a nonvolatile memory in the power-off mode. The conventional Ferroelectric DRAMs suffer from low endurance during read/write operations. This approach can remove such a degradation as the imprint. The ideal ferroelectric RAMs are also non-volatile, and low power DRAMs without refresh operation.

2.2 Embedded DRAM[4]

A data transfer rate of 6.4 GB/s with a 8Mb test DRAM chip was achieved. The bank modules, each with a capacity of 256 kb amplifier, are cascadably connected to form a 128-bit-wide, multi-bank DRAM macro. This chip is aiming at 3-D computer graphic engines. Moreover, multi-level flash memories will be important, in particular for large storage applications, which also result in low power consumption due to suppressed chip size. However this approach will put severer constraints on oxides.

3. SCALED MOS DEVICES

Due to the strong demand for lower power consumption in the nomadic age, the supply voltage is reduced to 3.3 -1.5 V, resulting in the reduction of hot-carrier effects. Thus, more attention must be paid to "substrate engineering" of device structures, such as the punch through stopper, to suppress the short-channel effects. In order to keep high performance under reduced supply voltage, it is important to simultaneously suppress Vth lowering and keep Vth low. Of course, the increase of subthreshold current due to low Vth must be overcome by circuits/architectures. The pocket structure provides low Vth and highly suppressed Vth lowering.

As the ultimate device structure of the substrate engineering method, much attention has recently been paid to thin film SOI device structures. Although crystal quality problems remain, thin film SOI technology may be able to provide new low cost fabrication processes, as well as higher performance and low power consumption due to smaller or negligible S/D capacitance. It will drastically change the isolation process and the memory cell process. In addition, the single electron devices provide very low power electronics and very reliable memory devices, which may lead to the ultimate flash memories.

4. LOW POWER ELECTRONICS

Various constraints associated with lowering voltage,

such as derivability degradation and the controllability of low threshold voltage, have not been solved, thus implying the need for new challenges to "low power electronics".

According to CMOS power dissipation eq.: $P = k C VDD^2 f + IDCVDD$, supply voltage (VDD), load capacitor (C), and subthreshold leakage current (IDC) should be reduced to suppress power dissipation. The first term is AC active and the second is DC standby power consumption. Here. new low voltage devices and circuits are discussed from the viewpoints of DRAM, subthreshod current, and post-CMOS circuits (pass transistor logics).

4.1 Low Power Circuits

i) Standby power reduction

DC current (subthreshold leakage current) is effectively reduced by applying switched-power-line schemes. In order to maintain high speed even in reduced supply voltages, Vth must be scaled down with supply voltage. However, the drastic (exponential) increase in suthreshold current occurs, resulting in increase of power consumption. There are use of thin film SOIs, which provide subthreshold coefficient as small as 65 mV/dec and low temperature operation to reduce subthreshold current. As circuits techniques, the following ones are proposed[5]: 1) Self-reverse-biasing scheme, 2) Switched-source-impedance scheme

As shown in Fig.4-1, a pMOS switching transistor is inserted between the power supply-line VCH and the driver transistor's common-source terminal VCHL. The channel width of switching transistor is designed to be comparable to that of the driver transistors. Thus, the switching transistor limits IDC in the standby mode, while maintaining high-speed performance in the active mode. The VCHL decreases in the standby mode by ΔV related to the subthreshold current in the pMOS transistors in the driver circuits. The ΔV acts as a self-reversing bias between the gate and source of the pMOS transistors. Therefore, the subthreshold current decreases exponentially. This scheme is considered to be effective for LSIs comparable to 256 Mb DRAMs.

In irregular logic circuits, on the other hand, the switched-source-impedance scheme is effective. This scheme reduces IDC in the standby mode in logic gates by inserting switching transistors between the source terminals of transistors in the subthreshold region and power supply lines, as shown in Fig.4-2. By combining the logic gates of Figs.4-2 (a)-(e), the switched-source-impedance scheme can be applied to any logic circuits as long as the voltages of its input signals in the standby mode are predictable. Furthermore, to reduce the subthreshold current in the active mode, the hierarchical-power-line scheme which divides high-density decoded iterative circuits into many blocks and to selectively supply power into many blocks in the active mode, has been proposed[6].

ii) Active power reduction

As low-power-circuit techniques, which maintain high performance even in power supply reduction, 1) light load-capacitance circuits such as pass transistor logics, 2) relaxation of the operation frequency by parallelism such as embedded memories, and 3) small-voltage-swing signal transmission have been proposed. As another novel approach, a charge recycle technique [7] is discussed, which halves the operating voltage by recycling the charge from one circuit block to the other.

The principle of the charge recycle refresh is shown in Fig.4-3, compared with the conventional scheme. Repeating these operations results in a data-line charging current that is about half the conventional charging current, and thus the small peak current can reduce the voltage bounce in the power supply line.

4.2 Post CMOS -- LEAP

A new circuit technology named LEAP (lean integration with pass transistors) was developed [8]. Pass-transistor circuits have an inherent advantage, that is, both charging and discharging can be done by a single transistor, leading to the smaller load capacitance. Therefore, complex functions are achieved with a small number of transistors. In contrast, both pMOS and nMOS are needed to charge and discharge the load capacitance in conventional CMOS. In actual ULSIs, however, pass-transistor logic has been used in a small portion of arithmetic macros. The major reason for this is that there is no established design methodology or tools for forming general logic functions. We cleared this hurdle by establishing the first top-down pass transistor logic design scheme called LEAP.

The function of a logic block is given in a hardware description language such as VHDL. Pass-transistor logic circuits are then synthesized by the new tool Circuit Inventor. Here, a binary decision diagram, BDD, is intensively used instead of conventional Boolean minimization, because the function of pass-transistor logic, selecting one of two data according to the control signal, is a "binary decision" itself and suits the BDD. The Circuit Inventor refers to this pass-transistor cell library, which consists of multiplexers. The unique feature of this library is that it does not include the more familiar cell functions, like NAND, or NOR. Those functions are replaced by the multiplexers. The netlist generated using the pass-transistor cells is used in automatic placement and router to produce mask layout patterns.

One important issue to be clarified before using pass transistors is whether they work under the lower supply voltages. The nMOS pass transistors are believed to have poorer low-voltage performance than CMOS circuits, which might raise doubt about future applicability. Although the delay becomes larger than that of the CMOS when we reduce the supply voltage without reducing the threshold voltage, in realistic situations, LEAP is always faster than CMOS. LEAP has been shown to be faster than CMOS if the supply voltage is 2.7 times larger than the threshold voltage, which has always been satisfied in real LSIs.

Benchmark Tests of a 4b Adder/Subtracter show that delay and power are improved by roughly 30-40 %. The total performance-cost ratio, which is defined as the product of these three figures, is three times as high as that of the conventional CMOS circuits.

5. METALLIZATION -- Cu, Low e, and CMP

An Al monolayer is limited in the region of 1 μm due to stress migration. After that, Al-rare metal multilayers have been used, but electromigration is a limiting factor near 0.2 μm. In that case, there is a mixed use of multi-layers and W. After that, Cu and grain-controlled Al will be important [9]. In terms of stressmigration, in the submicron region, monolayer AlSi and AlCuSi can not be used. Even Cu has poor stress migration reliability in the region less than 0.2 μm. Thus, layered Al and Cu are important. Metallization technology, including CMP (Chemical Mechanical Polishing), should be developed with application to logic circuits, as well as to memories, in mind. Furthermore, interlevel dielectric reliability and lower dielectric constant ε (< 3) will be needed to achieve low power and higher performance microprocessors.

6. CONCLUSIONS

An overview of new challenges to the coming GSI technology was discussed in terms of low power and low voltage in this paper. The key words are high performance, high reliability, and highly diversified GSI applications under low cost and low power with customer satisfaction in mind. These technologies will be able to open the real nomadic age at the beginning of 21st century. How can we manage these inconsistent trade-offs? We will have to cope with the new wave and a new paradigm, that are quite different from the simple down-scaling. Fortunately, such new user-oriented systems as game softwares and chips, and such multimedia systems as "Karaoke" have already been developed. These experiences encourage us to open the new GSI era. Also with new approaches to DA/CAD systems including virtual factories, as well as GSI technology, can we pave the way for intelligent GSIs in the 21st century.

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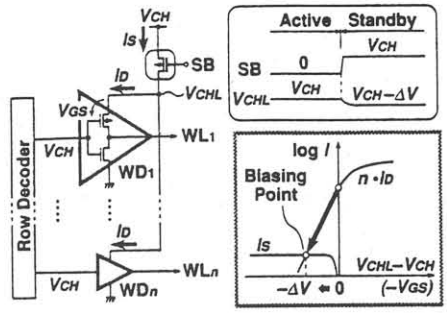

Fig. 4-1 Self-reverse-biasing circuit

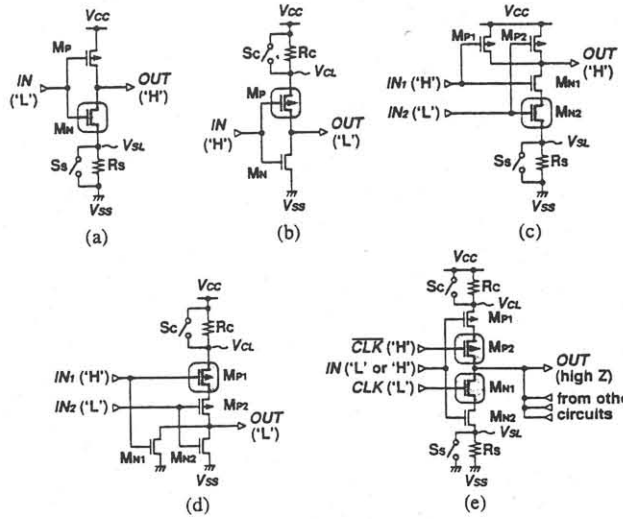

Fig. 4-2 Switched-source-impedanceCMOS circuits

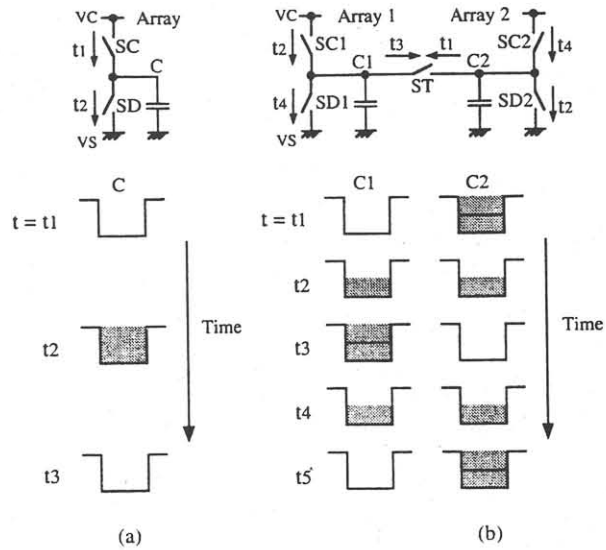

Fig. 4-3 Principle of charge recycle operation