Extended Abstracts of the 1996 International Conference on Solid State Devices and Materials, Yokohama, 1996, pp. 22-24

Proposal of Pseudo Source and Drain MOSFETs and Evaluation for 10-nm Gate MOSFETs

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We propose a Pseudo Source and Drain MOSFET (Ps-MOSFET) for investigating the electrical characteristics and physical phenomena in 10-nm gate MOSFETs. Since the Ps-MOSFET has an ultrashallow source/drain induced electrically, short-channel effects are expected to be suppressed in this structure. Numerical simulations are performed to confirm this, and satisfactory transistor operations of 10-nm gate Ps-MOSFETs are obtained. We also show that the direct source-drain tunneling current is not negligible in such short gate devices.

1 Introduction

There has been intensive research into 0.1-μm MOSFETs [1, 2] and the normal operations of 40-nm gate MOSFETs have been reported [3]. As the next step, it is important to characterize MOSFETs with a gate around 10-nm long. When the gate length is scaled down to this region, device characteristics may be affected by quantum mechanical effects. Therefore, investigating of the 10-nm gate MOSFET operations is important for estimating operation limitations in CMOS LSIs.

Recently, the 10-nm level lithography technique has been developed using the high-resolution EB resist, and 10-nm gate patterning is possible with this technique [4]. Besides that, for 10-nm gate transistor operations, ultrashallow source/drain junctions are required to prevent short-channel effects [5]. Moreover, the doping density in the source/drain regions must be sufficiently large to reduce a parasitic resistance. There has not been reported on fabrication techniques for such a junction.

Here, instead of a conventional MOSFET structure itself, we propose an alternative structure, a Pseudo Source and Drain MOSFET (Ps-MOSFET). A Ps-MOSFET has electrically induced ultrashallow source/drain regions which effectively prevent the short-channel effects. Therefore, if the ultrafine gate patterning were possible, ultrashort gate transistor operation could be achieved. Although this structure is not suitable for real applications, we can investigate physical phenomena in ultrashort gate MOSFETs without fabricating any ultrashallow junctions.

2 Device Structure and Operation Principles

Figure 1 illustrates a Ps-MOSFET and a channel potential at the surface. The Ps-MOSFET has a dual-gate structure in which the source and drain are positioned apart from the lower gate.

When a positive bias is applied to the upper gate, the source and drain are connected electrically through the induced channel. Transistor operation is possible as the channel under the lower gate is connected/disconnected by the lower gate voltage. The two channel regions separated by the lower gate can be regarded as a pseudo-source and a pseudo-drain. Since the junction depth of the regions is shallower than that of the diffusion layer formed by conventional techniques such as the ion implantation technique, we expect short-channel effects to be suppressed in this structure.

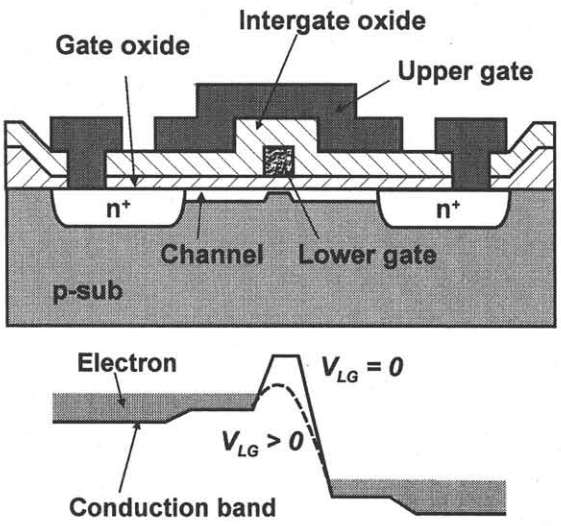

Figure 1: Schematic crosssection of a Pseudo Source and Drain MOSFET, and surface potential profile

We have preliminarily fabricated a 0.84-μm gate Ps-MOSFET to confirm the basic device operations. The substrate doping concentration (N_A) was 5×15 cm^{-3}, and the gate oxide layer thickness (t_{ox}) was 50 nm. The thickness of the intergate LPCVD oxide layer (t_{iox}) between a poly-Si lower gate and an aluminum upper gate was 20 nm.

Figure 2 shows the current-voltage characteristics of the fabricated device. Although the short channel effects are observed due to the small N_A and the large t_{ox}, MOSFET-like characteristics are obtained. Thus, the basic operation of Ps-MOSFETs has been confirmed

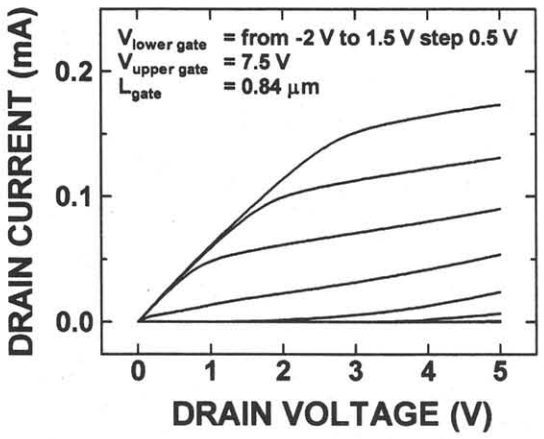

Figure 2: Current-voltage characteristics of preliminarily fabricated Ps-MOSFETs

in the preliminary device. A further reduction in gate length (down to the 10-nm scale) can be achieved using the 10-nm level lithography technique.

3 Calculation of Device Characteristics based on the Classical Drift-Diffusion Model

Prior to the actual fabrication of the 10-nm gate Ps-MOSFETs, the 10-nm gate device characteristics were evaluated using a 2-dimensional device simulator based on the classical drift-diffusion model. Although the drift-diffusion model is not strictly valid in such ultrashort gate devices, we used the simulator to obtain semi-quantitative information.

For a 10-nm gate transistor operation, the surface potential barrier beneath the lower gate has to satisfy the following two conditions. First, the barrier height should be large enough to suppress a leakage current from a source to a drain. Second, the barrier width should be as short as the length of a lower gate. The second condition is equivalent to the condition that the pseudo-source/drain regions should be sufficiently close to the lower gate.

These two conditions depend mainly on the lower gate oxide thickness (t_{ox}), the intergate oxide thickness (t_{iox}), and the substrate doping concentration (N_A). The first condition is satisfied with a small t_{ox} and a large N_A. A small t_{ox} decreases the influence of the upper gate voltage on the electrostatic field beneath the lower gate, and a large N_A prevents the extension of the depletion layers associated with the pseudo-source/drain regions.

The second condition is satisfied with a small t_{iox} and a small N_A. When t_{iox} is small, the positions of pseudo-source/drain regions are laterally close to the lower gate. However, if N_A is too large, the carrier concentrations in the pseudo-source/drain regions beside the lower gate are suppressed. Therefore, a small N_A is desirable in this case.

In order to satisfy both conditions as discussed above, the substrate doping concentration (N_A) should be optimized. We therefore calculated potential barrier dependencies on several N_As.

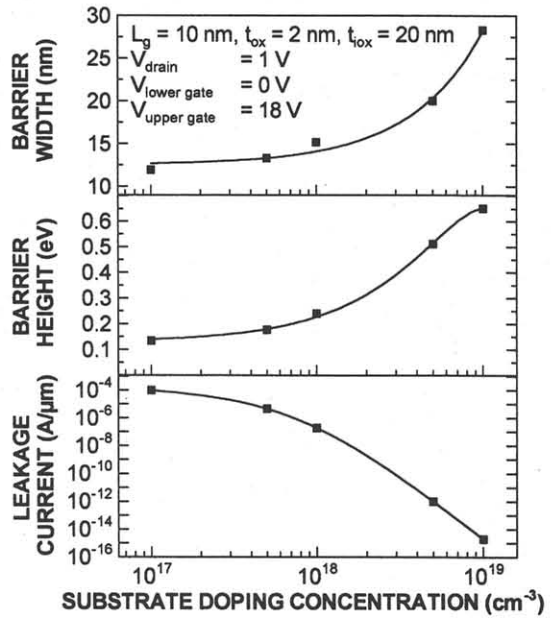

Figure 3: Surface potential barrier and leakage current as a function of the substrate doping concentration

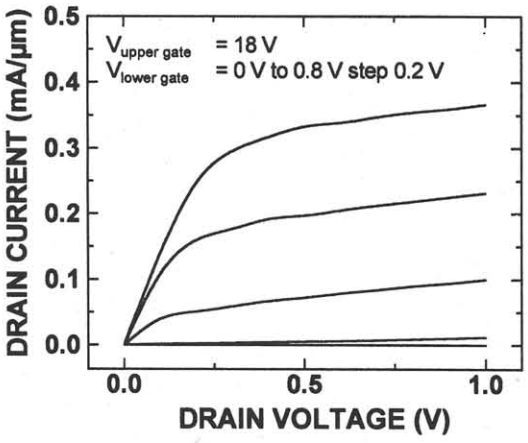

Figure 4: Calculated current-voltage characteristics of Ps-MOSFETs

Figure 3 shows a potential barrier and a leakage current between a source and drain as a function of the substrate doping concentration. In this calculation, the following parameters are used: $t_{ox} = 2$ nm, $t_{iox} = 20$ nm, $L_{gate} = 10$ nm, $V_{lower\ gate} = 0$ V, $V_{upper\ gate} = 18$ V, $V_{source} = 0$ V, $V_{drain} = 1$ V. In the region of $N_A < 1 \times 18$ cm^{-3}, although the barrier width is as small as 12 nm, the leakage current is considerably large due to the small barrier height.

However, in the region of $N_A > 1 \times 18 cm^{-3}$, although the leakage current is suppressed due to the large barrier height, the barrier width abruptly increases with the increase in N_A. Therefore, the optimized substrate doping concentration is estimated to be around 1×10^{18} cm^{-3} and, in this case, a potential barrier 15-nm wide and 250-mV high is obtained.

Figure 4 shows the calculated current-voltage char-

acteristics of the optimized structure discussed above. Although a slight short-channel effect is observed in the saturated region, transistor operation controlled by the lower gate is obtained.

Figure 5 shows the drain current as a function of the lower gate voltage. Although the cut-off current is not perfectly suppressed due to the short-channel effects, the gate modulation in the drain current is obtained by over three orders of magnitude.

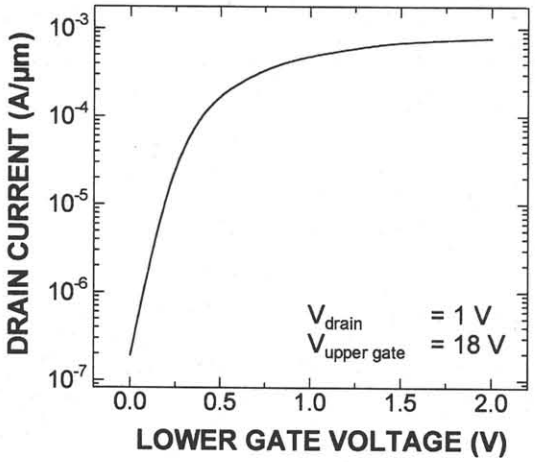

Figure 5: Calculated drain current as a function of the lower gate voltage

4 Quantum Calculation of the Source-Drain Direct Tunneling Current

In such a short gate device, several quantum effects may appear in the electrical characteristics. In particular, the direct source-drain tunneling current is a serious problem, because the current degrades the cut-off characteristics of the device. Therefore, it is important to estimate the direct tunneling current. For this purpose, 1-dimensional quantum mechanical calculations were performed using the potential and electron profiles calculated by the 2-dimensional device simulation.

Since the channel potential and the electron density are not constant in the vertical direction, both profiles are divided into several elements with a width of 0.2 nm where their variation in the vertical direction is neglected. The 1-dimensional calculation is performed for individual elements. After that, the total tunneling current was evaluated by summing up the current in all elements.

Figure 6 shows the calculated direct source-drain tunneling current and the thermal leakage current under the cut-off condition ($V_{lower\ gate} = 0V$). The direct tunneling current has an order of magnitude comparable with that of the thermal cut-off current. Since the direct tunneling current is supposed to degrade the cut-off characteristics of the 10-nm gate MOSFETs, it is important to carry out experimental studies using the 10 nm-gate Ps-MOSFET structure.

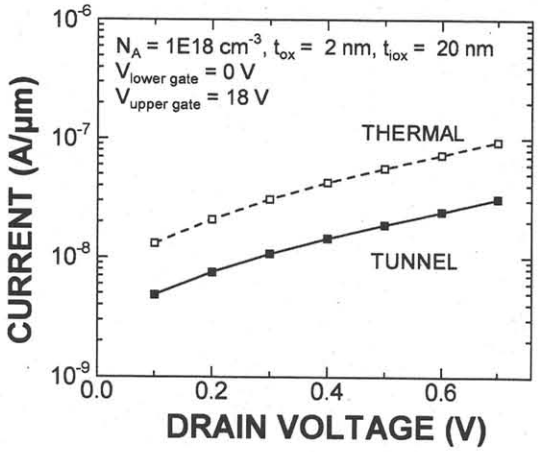

Figure 6: Calculated source-drain direct tunneling current and thermal leakage current under the cut-off condition as a function of the drain voltage

5 Conclusion

A Ps-MOSFET structure was proposed for investigating device characteristics and physical phenomena in 10-nm gate MOSFETs. Transistor operations of 10-nm gate Ps-MOSFETs with an optimized substrate concentration ($1 \times 10^{18}\mathrm{cm}^{-3}$) were confirmed by using a 2-D simulation. We also found that that the source-drain tunneling current had an order of magnitude comparable with that of the thermal cut-off current.

Acknowledgments

We would like to thank to H. Rangu for his encouragement. Part of this work was performed under the management of FED as a part of the MITI R&D program (Quantum functional Device project) supported by NEDO.

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