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Self-Aligned Control of Threshold Voltages in 0.1 μm nMOSFETs

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We propose a new method for controlling threshold voltages of 0.1 μm MOSFETs. We used a large-angle and low-energy tilted ion implantation after polysilicon gate formation. We fabricated 0.1 μm nMOSFETs using this process and succeeded in suppressing short channel effects. With the increase in the dose of tilted ion implantation, larger reverse short channel effects appeared. This is attributed to the increase in the concentration of channel impurity for shorter gate length. Hence control of threshold voltages self-aligned to the gate length is possible.

1. Introduction

The fluctuation of device characteristics caused by the variation in the fabricated gate length is a critical issue for realizing ULSI devices using 0.1 μm MOSFETs. To solve this problem, we propose a new method to control threshold voltages in 0.1 μm MOSFETs. As shown in Fig. 1, we use a large-angle and low-energy tilted ion implantation (II) after polysilicon gate formation. For a long gate, the impurity concentration under the center of gate is low, because tilted II is masked by the gate. However, for a short gate, the impurity concentration becomes high, because the tilted IIs from two directions overlap under the center of gate. Hence the increase in the impurity concentration self-aligned to the gate length occurs as shown in Fig. 2.

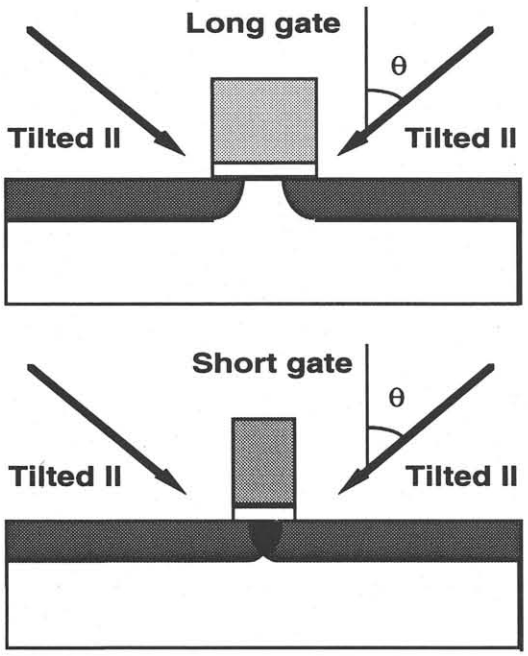

Fig. 1. Schematic representation of our method for controlling threshold voltage.

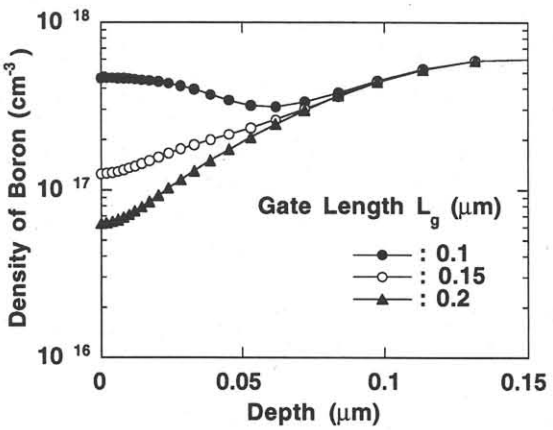

Fig. 2. Depth profile of boron under center of gate simulated by SUPREM-4 for each gate length. Tilted II of boron (θ=45°) at 10 keV with a dose of 4×10^{12} cm^{-2} is assumed.

2. Device Fabrication

The devices were fabricated by the conventional LDD-nMOS process except for the tilted II after gate etching. The conditions are shown in Table 1. The large tilt angle (θ=45°) and low energy (10 keV) II of boron was used. This method is different from the conventional halo punchthrough stopper or TIPS[1][2], because we aim to change the channel impurity concentration by tilted II. The II processes before gate oxidation form the retrograde well as shown in Fig. 2 (profile for L_g=0.2 μm). The gate oxide thickness is 3.5 nm. After gate etching, tilted II and LDD II (As) were done. Then the 60 nm oxide sidewall spacer was formed and deep source/drain II (As) was carried out. The final anneal was RTA at 1000°C for 10 seconds.

Sample	Energy (keV)	Dose (cm^{-2})
1	---------	---------
2	10	4×10^{12}
3	10	7×10^{12}
4	10	1×10^{13}
5	30	4×10^{12}

Table 1. Conditions for tilted II at $\theta=45^{\circ}$ in each sample.

3. Results and Discussions

Figure 3 shows the subthreshold I-V characteristics of Sample 2 with a gate length L_g=0.15 μm. We obtained good turn-off characteristics and leakage currents for negative gate voltages were lower than Sample 1 having no tilted II.

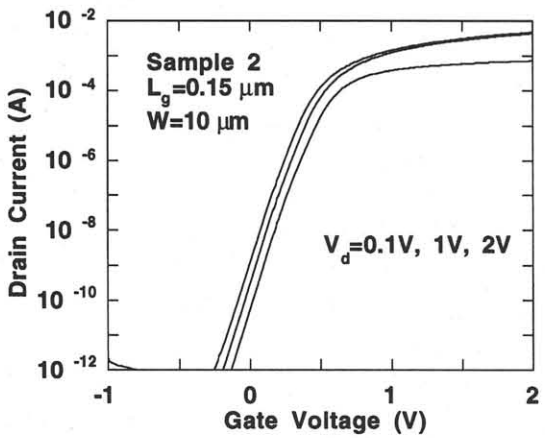

Fig. 3. Subthreshold I-V characteristics of Sample 2 at V_d=0.1 V, 1 V, and 2 V. Gate length L_g is 0.15 μm.

Figure 4 shows the threshold voltages V_{th} of the samples having different doses of boron by tilted II at 10 keV. In this figure, the gate length L_g is defined as the length of gate polysilicon measured by SEM. The lowering of V_{th} in Sample 2 is sufficiently suppressed, while Sample 1 suffers from the short channel effect. With the increase in the dose of tilted II, a larger reverse short channel effect (RSCE) appears.

Similar RSCE was obtained from simulations, as shown in Fig. 5. In this simulation, the result of process simulation by SUPREM-4 (Fig. 2) was introduced into the 2-D device simulator, and we calculated the subthreshold characteristics by a drift-diffusion model. Although the V_{th} lowering is a little larger in Fig. 4, the agreement between the experimental and simulation results is reasonable. Hence the RSCE in these devices is attributed to the increase in the channel impurity concentration for short L_g, which is intentionally caused by tilted II. It is not due to the redistribution of boron by diffusion processes[3][4].

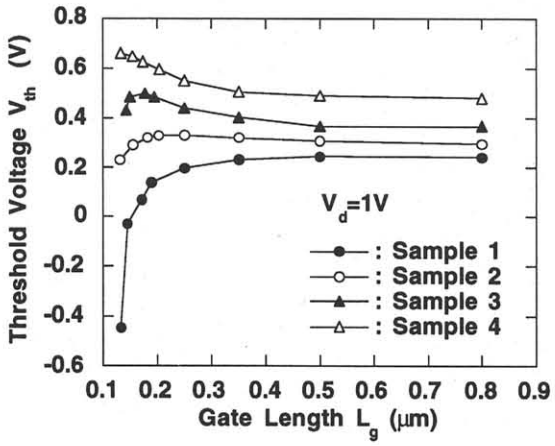

Fig. 4. Experimental threshold voltage V_{th} at V_d=1 V versus gate length L_g for samples with different doses of boron at 10 keV.

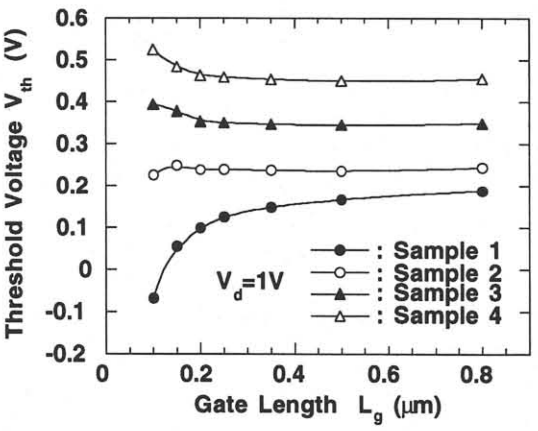

Fig. 5. Simulated threshold voltage V_{th} at V_d=1 V versus gate length L_g. The result of process simulation by SUPREM-4 (see Fig. 2) was used in the 2-D device simulation. Assumed conditions for tilted II and other processes were same as the fabricated samples.

In Fig. 6 we compared the experimental V_{th} values in Samples 2 and 5. The energy of tilted II used for Sample 5 is higher, and is close to the condition for punchthrough stopper formation[1][2]. Sample 5 shows a large RSCE, although the dose is same as Sample 2. This shows a higher channel impurity concentration in Sample 5 for short L_g. However, since V_{th} lowering for L_g near 0.1 μm is larger in Sample 5, variation in the fabricated gate length results in larger V_{th} fluctuation.

Figure 7 shows the drain current I_d in Samples 2 and 5. The I_d is larger in Sample 2 for a short L_g because of the RSCE in Sample 5, although I_d for a long L_g is almost the same. These results show that low-energy tilted II is favorable for our method.

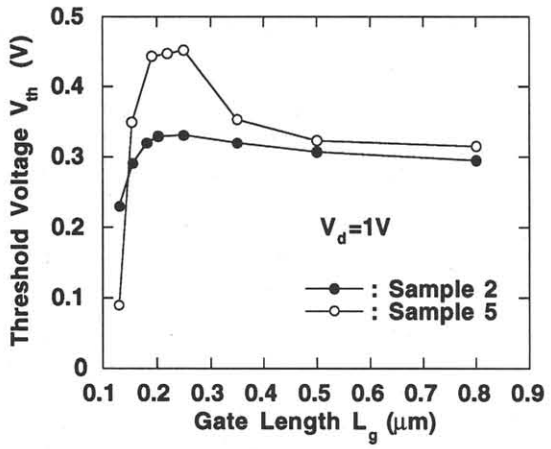

Fig. 6. Experimental threshold voltage V_{th} at V_d=1 V versus gate length L_g for samples with different II energies.

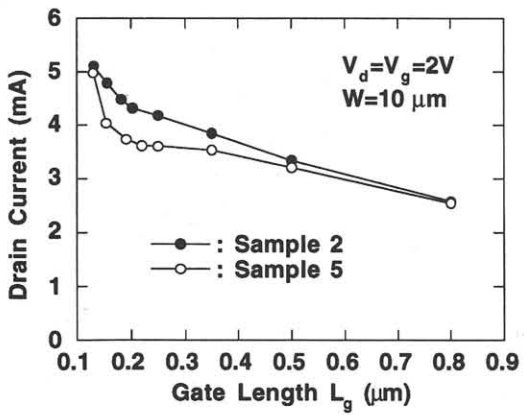

Fig. 7. Experimental drain current I_d at V_d=V_g=2 V in Samples 2 and 5.

4. Conclusions

We proposed a new method for controlling V_{th} of 0.1 μm MOSFETs. The large-angle and low-energy tilted II after polysilicon gate formation can change the impurity concentration in the channel, which allows V_{th} control self-aligned to L_g. The effectiveness of our method was confirmed by both experiment and simulation. This method is more promising than the formation of a punchthrough stopper to suppress V_{th} fluctuations in MOSFETs with L_g=0.1 μm.

Acknowledgments

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References

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