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Three-Terminal Silicon Esaki Tunneling Device

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Negative differential conductance based on lateral band-to-band tunneling is demonstrated for the first time in a three-terminal Si Esaki tunneling device. The device is fabricated with the current Si ULSI process, taking care of the gate edge region to reduce the excess tunneling current that flows over some intermediate states. It is observed that the forward biased band-to-band tunneling current is largely controlled by the gate bias which modulates the tunneling barrier width. The three-terminal Si Esaki tunneling device will be a promising functional device candidate as the post-CMOS devices in future Si ULSI.

1 Motivation

Low-power, high-speed and multi-functionality are key factors towards the future Si ULSIs. Recently, the physical limitations of Si MOSFETs have been discussed as the device dimensions are scaled down to 0.1 μm and below. Therefore, novel Si devices which operate normally in ultra-small structures are needed to construct the future ULSIs with feature sizes of less than 0.1 μm. Negative differential conductance (NDC) devices based on forward biased interband tunneling have been investigated because of the versatile functionality [1].

The objective of this paper is to report the first experimental observation of the NDC characteristics in a three-terminal Si Esaki tunneling device, in which the active device length is less than 0.01 μm. To our knowledge, the structure of the three-terminal tunneling device was originally studied for the sub-band spectroscopy by J. J. Quinn et al. [2], named a surface tunnel transistor (STT) by T. Uemura et al. who have shown the NDC characteristics in the compound semiconductor heterostructure [3]. However, considering that the silicon is the industry standard for electronic devices, further device applications can be expected utilizing Si tunneling devices. Physically, the silicon is more attractive due to higher density of states in tunneling. Therefore, we focused on the lateral band-to-band tunneling in the Si STT structure under the forward bias condition.

2 Device Structure

The Si STT structure differs from a conventional MOSFET only in that the doping of the source region is opposite to that of the drain region, as illustrated in Fig. 1. The operation principle of this tunneling device is the same as that of the Esaki diode [1]. When a positive gate bias is applied to induce a two-dimensional electron gas (n^+ channel) in the surface of a p-type Si substrate, the tunneling barrier is formed in the system of the n^+ channel/p^+ drain junction. It is expected that the device will display the NDC characteristics at a forward drain bias, as the Esaki diode does. The tunneling current varies with the gate bias condition, because the surface electron density, or the tunneling barrier, is controlled by the gate bias. On the other hand, conventional p–n junction characteristics appear at the "off" gate bias, where no current flows at the low drain biases. Therefore, the three-terminal Si tunneling device inherently has the functions of both the gate-controlled Esaki diode and a simple switching element below a drain bias of 0.5 V. Also, it should be noted that the punch-through, which is unavoidable in conventional MOSFETs, is not present in the STT structure.

3 Fabrication

The key point of the fabrication process in our device was to take care of the gate edge region in terms of the following items: (i) the field oxide edge, (ii) the field ion-implantation, and (iii)

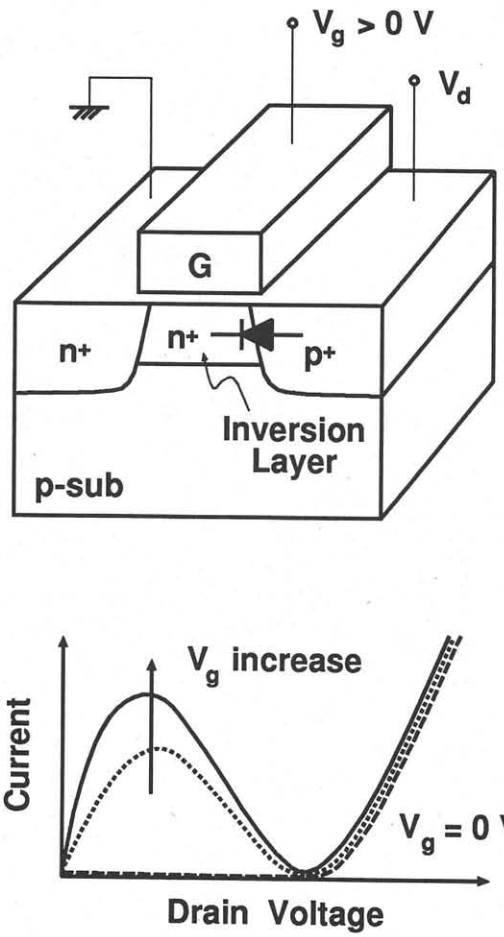

Figure 1: Schematic view of three-terminal Si Esaki tunneling device structure and its characteristics predicted by a simple tunneling model.

the gate RIE. A severe mechanical stress around the LOCOS field oxide edge is considered to result in a large amount of defect generation. The defects work as intermediate states, which significantly increase the excess tunneling current and degrade the NDC characteristics [4]. In fact, the NDC characteristics were not observed in the Si tunneling devices which we fabricated with the conventional LOCOS isolation process. Furthermore, the removal of the defects induced during the process of (ii) and (iii) is very important to improve the NDC characteristics.

The device was fabricated on a p-type (100) Si wafer. The substrate impurity concentration was about 3×10^{15} cm^{-3}. The field oxide thickness was 25 nm which was formed by dry oxidation at 750 °C. There was no field ion-implantation for creating a p^- layer underneath the field oxide. The gate oxide layer of 5 nm was formed on the Si surface to induce many electrons by the low gate biases. The gate RIE defects were relaxed by dry oxidation after the gate patterning. It was followed by ion-implantation for creating the p^+/n^+ regions to achieve the sudden profiles. The ion-implantation condition for the p^+ region was at an energy of 60 keV and a dose of 5×10^{15} cm^{-2}. The ion-implantation condition for the n^+ region was at an energy of 30 keV and a dose of 2×10^{15} cm^{-2}. The annealing conditions for the p^+/n^+ impurity activation were at 800 °C for 30 min. The final junction depths of the p^+ and n^+ regions were calculated to be 0.15 μm and 0.1 μm by the device simulation, respectively. It was confirmed that the leakage current between the adjacent devices is negligible in spite of the thin field oxide layer.

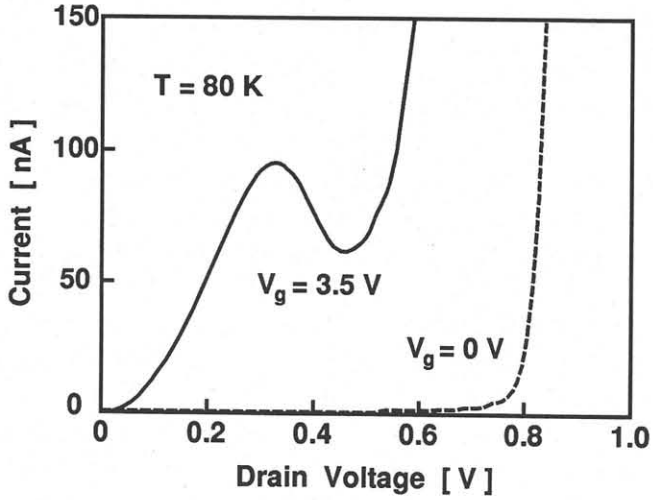

Figure 2: Negative differential conductance at 80 K in Si STT structure. Gate length is 0.6 μm and gate width is 5 μm. Oxide thickness is 5 nm. It is observed that the current is largely controlled by the gate bias.

4 Results and Discussions

We have clearly observed the NDC characteristics at 80 K at a gate bias of 3.5 V in the Si STT structure, as shown in Fig. 2. The gate length and width are 0.6 μm and 5 μm, respectively. The effective gate length is estimated to be nearly 0.4 μm, considering the lateral impurity diffusion in the source/drain regions. The current modulated by the gate bias was weakly dependent on the temperature, which confirms that the current results from tunneling. The peak-to-valley ratio was 1.5 and the peak current density was nearly 20 nA/μm that corresponds to 20 A/cm^2, assuming that the effective depth of the tunneling junction is about 0.1 μm. The peak current density is quite a reasonable value, compared to the previous experimental work on the Si Esaki diode [4]. It is expected that higher peak current density will be obtained

by achieving more abrupt p^+ doping profile.

This is the first demonstration of the Esaki tunneling effect in the three-terminal Si tunneling device. The "off" current at the gate bias of 0 V was smaller than 1 pA/μm at the drain bias of 0.3 V, where the peak current appears at a gate bias of 3.5 V, indicating a great controllability of the tunneling current. This tunneling current was obtained at drain bias lower than 0.5 V, which significantly reduces the power-supply voltage of the device operation. Moreover, the physical length of the device can be reduced dramatically, because the tunneling distance controlled by the gate bias is less than 0.01 μm. In such an ultra-small device structure, a large transconductance can be obtained with only a very low capacitance. Therefore, the three-terminal Si tunneling device is a promising candidate for the low-power, high-speed and multi-functional devices in the sub-0.1 μm Si ULSI.

Figure 3 shows the dependence of the tunneling characteristics on the gate bias, where the base current level is shifted for clarity. The gate voltages are varied from 0 V to 3.5 V in 0.1 V steps. The "hump" current begins to be observed at the gate bias of $\sim$ 2 V, which is interpreted as the band-to-band tunneling current. The band-to-band tunneling current becomes significant with increasing gate bias and brings about the NDC characteristics above $\sim$ 3 V.

The induced electron density in the surface inversion layer at the gate bias of 3.5 V was estimated to be 1.8×10^{13} cm^{-2} from the channel capacitance measurement. It corresponds to 5×10^{19} cm^{-3} in n^+ concentration, assuming that the inversion layer width is 3 nm [5]. Hence, the depletion layer width of the tunneling junction was calculated to be 0.007 μm, using the p^+ impurity concentration of 5×10^{19} cm^{-3} from the simulation results. This value is very reasonable as a tunneling distance.

It is considered that the defects at the Si/SiO_2 interface bring about an increase in the excess tunneling current, because the defects around the field oxide edge are almost eliminated in the present Si STT structure. It is hoped that the reduction of the interface states at Si/SiO_2 decreases the valley current of the NDC characteristics. Therefore, the control of the Si/SiO_2 interface quality is very important to obtain excellent NDC characteristics. Also, the impurity optimization can improve the device characteristics in order for the band-to-band tunneling to occur apart from the Si/SiO_2 interface instead of at the interface.

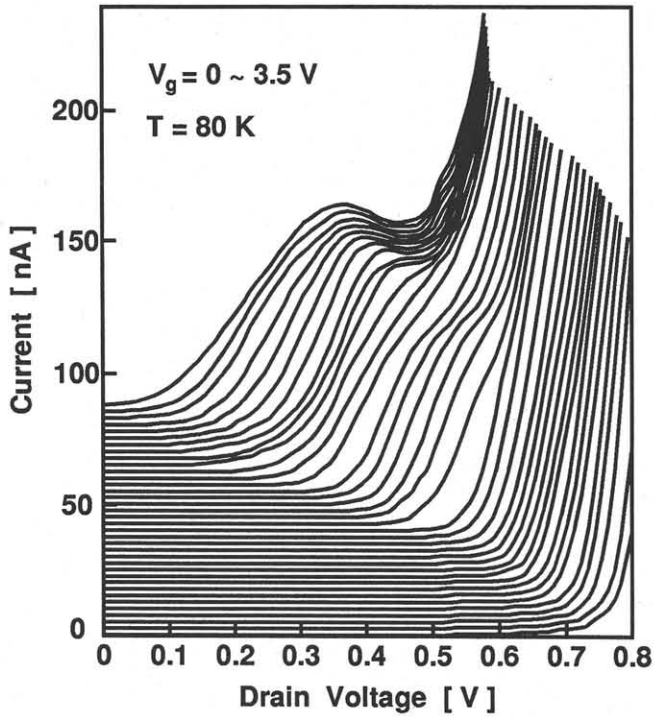

Figure 3: Dependence of tunneling characteristics on gate bias. The base current level is shifted for clarity. Gate voltages are varied from 0 V to 3.5 V in 0.1 V steps.

5 Conclusion

Negative differential conductance based on the Esaki tunneling effect has been demonstrated for the first time in a three-terminal Si tunneling device. This functional device will be more robust than the recent quantum effect devices and become versatile and promising as the post-CMOS devices in the sub-0.1 μm Si ULSI.

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