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Channel Doping Engineering with Indium as an Alternative p-Type Dopant

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We have investigated the properties of indium for channel doping engineering. We have fabricated 0.1μm Super-Steep-Retrograde(SSR) channel nMOSFETs and buried channel pMOSFETs with indium counter doping layer. It is found that : (1) In is a promising candidate as a channel dopant when it is implanted into sub-surface with relatively high energy and its steep profile is maintained throughout the full process of SSR nMOSFETs. (2) however, it is not practical as a dopant for the near p-type conduction layer such as buried channel or p^- LDD in pMOSFETs due to incomplete ionization and high diffusivity in oxide.

Introduction

As the dimension of CMOS devices have been scaled into deep submicron regime, more strict process conditions are required in channel doping. To obtain the low threshold voltage and suppress the short channel effect, super steep retrograde(SSR) channel doping is quite effective in surface channel MOSFETs. For buried channel pMOSFETs, the only way to achieve this goal is to form a ultra shallow counter doped layer on the n-well surface. To the meet above requirements, dopants should have high atomic mass, small diffusivity and sufficient solubility in silicon.

It is relatively easy to make n-type SSR channel profile or shallow junction due to the existence of the n-type dopant with high atomic mass and small diffusivity such as arsenic(As) and antimony(Sb). In p-type layer, however, most widely used p-type dopant, boron(B), is difficult to form such structures because of its high diffusivity. Gallium (Ga), another element of group III, also has very high diffusivity. But, indium (In) has a possibility due to its high atomic number and low diffusivity[1]. Fig 1 shows the diffusivity of In vs. temperature compared with boron. The diffusivity of In is about one order of magnitude lower than that of boron. It has been shown in several papers[2-4] that nMOSFETs with In have more scale-down capability than that with boron. Along the same line, it appears that buried channel pMOSFETs might be scaled down further if In is used in counter doping instead of boron.

In this work, we investigate the properties of In by fabricating surface channel nMOSFETs and buried channel pMOSFETs using In as a channel dopant and suggest the possibilities of In as channel dopant.

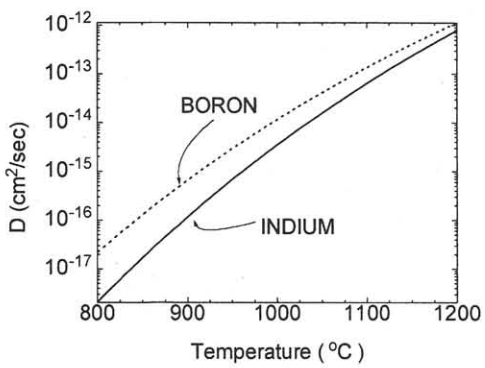

Fig.1. Diffusion coefficients of In and B vs. temperature in silicon[1].

Device Fabrication

Fig 2(a) and 2(b) show the schematic cross section of nMOSFET and BC pMOSFET. Table 1 shows the key process parameters. The gate oxide thickness is 4.0nm and n^+ poly silicon gate is used in both pMOSFET and nMOSFET. The nMOSFET has SSR channel profile by In implantation with energy of 130keV. Fig 3 shows as-implanted profile of In compared with BF_2. In has steeper profile than boron. Counter doping in the BC pMOSFET was carried out using the low energy implantation of In. As implanted layer was used as a punchthrough stopper. The gate electrodes were drawn by the electron beam writing. After the LDD formation using low energy ion implantation, the side wall spacer of 100nm was formed. The annealing after the source/drain implantation was accomplished by 1050 °C, 10's rapid thermal annealing and 800°C, 60min. by furnace annealing.

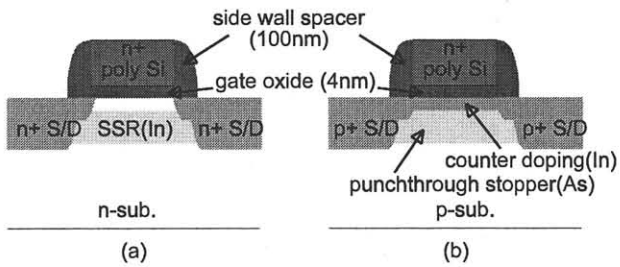

Fig2. Schematic cross section of SC nMOSFET(a) and BC pMOSFET(b).

Table1. Key process parameters of nMOSFET and pMOSFET

	SC nMOSFET	BC pMOSFET
Gate oxide	4nm	4nm
V_T adjust	In, 130keV $1x10^{13}cm^{-2}$	In, 15keV $1\text{-}6x10^{13}cm^{-}$
Punch through stopper	-	As, 130keV $1x10^{13}cm^{-2}$
Spacer	100nm, TEOS	100nm, TEOS
Anneal	1050°C, 10s 800°C, 60min.	1050°C, 10s 800°C, 60min.

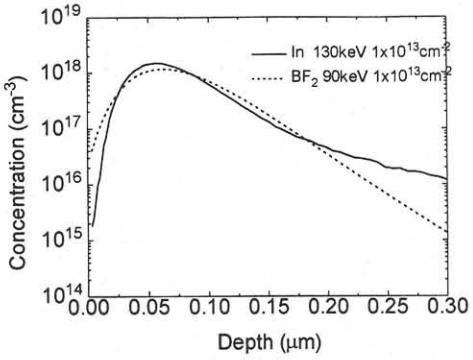

Fig. 3. Comparison of as-implanted doping profile of In with implantation energy of 130keV with that of BF_2 with implantation energy of 90keV.

Result and Discussion

Fig. 4 shows I-V characteristics of fabricated 0.1μm SSR nMOSFET using In implantation with energy of 190keV and dose of $1x10^{13}cm^{-2}$ as channel dopant. The saturation current is 484μA/μm at $V_{DS} = V_{GS} = 2V$ with $V_T = 0.34V$ and DIBL is retained within 70mV. Subthreshold swing of less than 90mV/decade and off-state current of less than 400pA/μm are obtained. Thus, In maintained the steepness of as-implanted profile during the annealing process. By using drain avalanche hot carrier(DAHC) injection test, the maximum allowable supply voltage to insure 10-year device lifetime was calculated as 2.26V(Fig. 5). This shows that deep implanted In channel does not degrade oxide and MOSFET reliability.

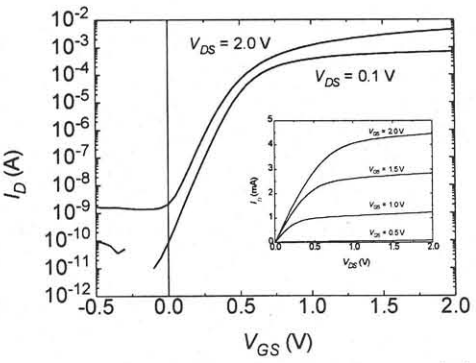

Fig. 4. Subthreshold and I_D -V_D characteristics. $L_{GATE} = 0.15\mu m$, $T_{ox} = 40Å$, $W_{eff} = 0.96\mu m$.

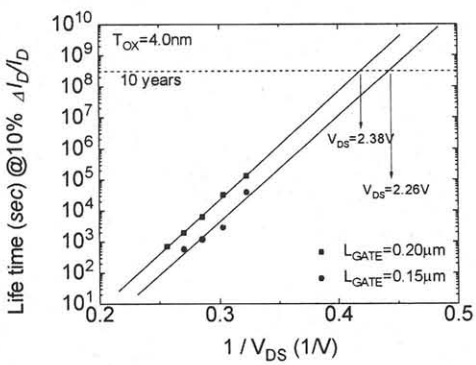

Fig 5. Hot electron life time versus supply voltage.

Fig. 6 shows threshold voltage variation as a function of implantation dose in buried channel pMOSFETs. The channel doping layer is formed by In implantation with energy of 15keV. The threshold voltage is too high and independent of In implantation dose.

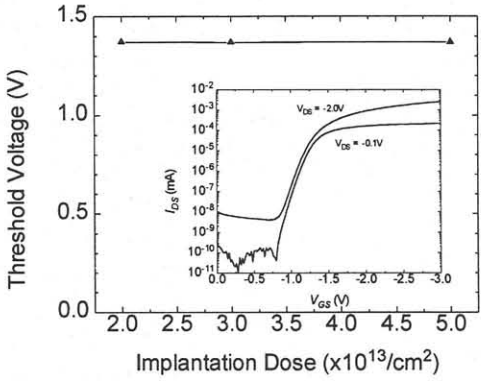

Fig. 6. Threshold voltage versus channel implantation dose of In in buried channel pMOSFET. The inset shows the subthreshold characteristics of a BC pMOSFET with $3x10^{13}cm^{-2}$ In implantation dose.

Confronted with somewhat unexpected result, we have carried out a detailed analysis on the properties of indium as a dopant in the counter doping layer. Since In has a relatively deep-lying energy level(0.155eV) in silicon, the carrier concentration and the electrically active dopant concentration are different even at room temperature. Fig 7. shows doping profile of 130keV, $1\times10^{13}cm^{-2}$ In, measured by three different techniques (SIMS, C-V, spreading resistance). C-V measurements can extract electrically active dopant concentration, but spreading resistance method extracts only carrier concentration. In Fig. 7, C-V and SIMS yield a very similar peak concentration, but carrier concentration measured by spreading resistance is only about 10% of active dopant concentration due to incomplete ionization.

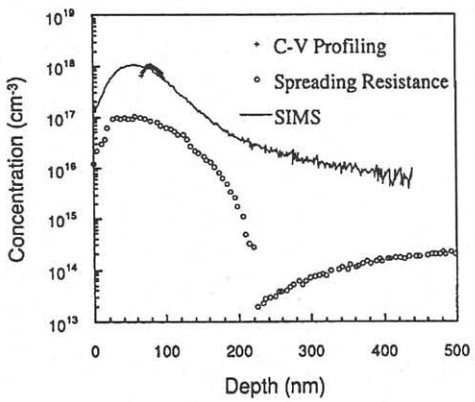

Fig. 7. Comparison of various profile measurement methods.

High diffusivity of In in oxide and segregation behavior at silicon-oxide interface introduce another problem in maintaining high surface doping level throughout the full device fabrication process. Fig. 8 shows the as-implanted and annealed doping profile. While the dose is more or less the same after 900°C, 60min. annealing in high energy implanted case, only 20% of the implantation dose remained after 900°C, 60min. anneal in low energy implantation. Thus, we can estimate that a significant amount of In is lost through oxide diffusion and/or segregation.

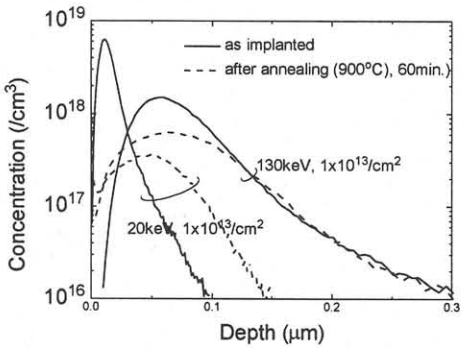

Fig. 8. Comparison of diffusion characteristics of In as different implantation energy.

In order to evaluate the impact of these In properties on the I-V characteristics of surface channel nMOSFETs and buried channel pMOSFETs, we have performed device simulation with MEDICI. For nMOSFET, we have used the same device/process parameters as in Table 1. For pMOSFETs, we have simulated two channel implantation case - one has relatively high remaining dose ($1x10^{13}$ cm^{-2}) and the other has low remaining dose ($5x10^{12}cm^{-2}$). Fig 9 shows the subthreshold characteristics of nMOSFETs. In nMOSFETs, In can be fully ionized because the Fermi level is far away from the acceptor level in the depletion region. As shown in Fig.9, subthreshold characteristics with incomplete ionization model are very similar to those with complete ionization model. In buried channel pMOSFETs, however, the simulation results are significantly different from that of nMOSFETs in subthreshold region when incomplete ionization model is used. As shown in Fig. 10, for the higher dose case, anomalous subthreshold characteristics near the threshold voltage has been observed due to incomplete ionization. For the lower dose case, larger threshold voltage and subthreshold characteristics similar to Fig. 5 have been observed mainly due to insufficient counter doping. From this result, we can conclude that low energy implantation of indium for ultra shallow p-layer is impractical not only due to incomplete ionization but also due to the severe loss of In at the surface.

Conclusion

We have fabricated nMOSFETs and BC pMOSFETs with 0.1μm channel length using In as channel dopant. For SSR nMOSFETs In is a promising candidate as a channel dopant since it is implanted into sub-surface with relatively high energy and its steep profile is maintained throughout the full process. For the near surface p-type conduction layers such as counter doping layer or p^- LDD of pMOSFETs, incomplete ionization and high diffusivity in oxide make it quite difficult to use In as a dopant.

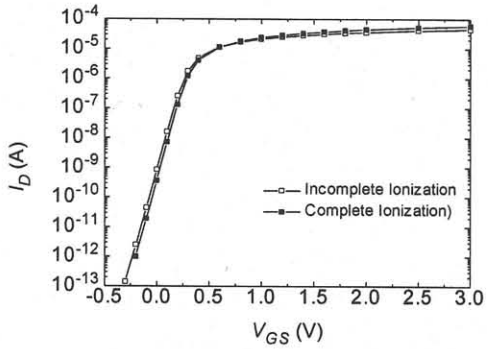

Fig. 9. Simulation result of subthreshold characteristics using incomplete ionization model of In in buried channel nMOSFET.

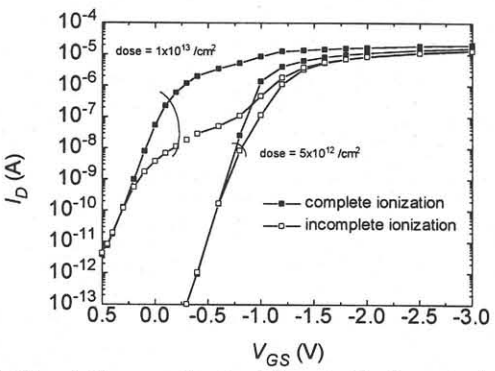

Fig. 10. Simulation result of subthreshold characteristics using incomplete ionization model of In in buried channel pMOSFET.

Acknowledgment

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