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Influence of Ion Energy on Carrier Activation and Source/Drain Parasitic Resistance in Low-Energy Ion Implantation for 0.15-μm MOSFETs

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Low-energy ion implantation was investigated in detail as a method of forming shallow and low resistance source/drains (S/Ds) for 0.15-μm MOSFETs. Rapid thermal annealing was found to be essential for obtaining diffused layers with low sheet resistance when the ion energy was decreased to 10 keV. Moreover, an increase in S/D edge resistance was observed in the fabricated MOSFETs. Thus, a relatively high implantation dose is necessary to obtain S/D diffused layers with low parasitic resistance.

I. Introduction

The formation of an ultra-shallow diffused layer with a depth of less than 50 nm is essential for 0.15-μm MOSFETs[1]-[2]. To obtain an ultra-shallow diffused layer by ion implantation, the ion energy should be lowered to reduce the ion projection range. The source/drain (S/D) parasitic resistance should also be lowered for high-performance operation. Thus, the electrical characteristics of ultra-shallow diffused layers need to be clarified. However, there have been no detail reports concerning ultra-shallow diffused layers fabricated by low-energy ion implantation. In this paper, we report on the influence of implantation energy on the carrier activation and sheet resistance, and on the S/D parasitic resistance of 0.15-μm MOSFETs.

II. Influence of Ion Energy on Carrier Activation and Sheet Resistance

Figure 1 shows the carrier activation ratio, defined as the sheet carrier concentration divided by implantation dose, of samples implanted using As or BF_2 with the ion energy ranging from 10 to 30 keV. The implanted doses were 1×10^{14} or 5×10^{14} cm^{-2}. Post-implantation annealing was carried out at 950 ℃ for 10 seconds (RTA) or at 800 ℃ for 10 minutes (FA). The carrier activation ratio of the RTA samples was higher than that of the FA samples in all cases. In particular,

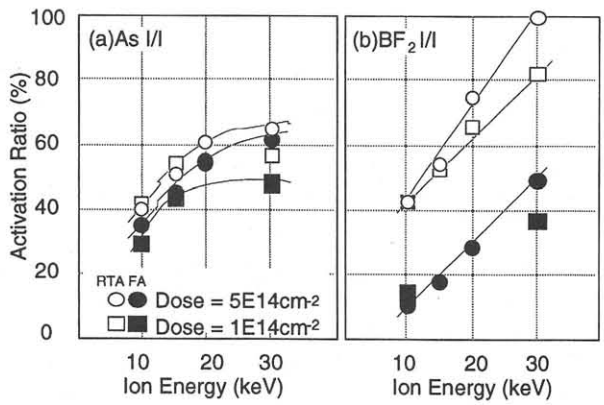

Fig. 1 Dependence of carrier activation ratio on the ion energy. (a) As ion implantation, (b) BF_2 ion implantation

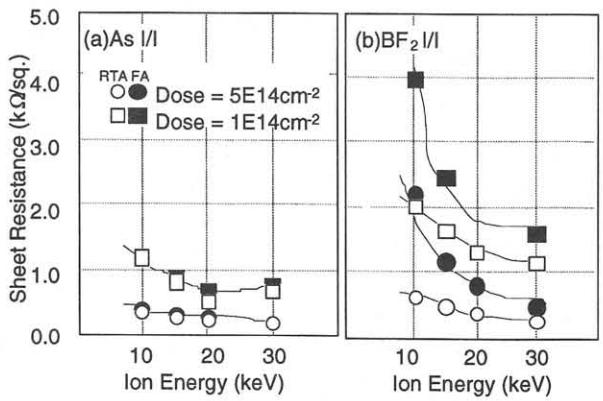

Fig. 2 Dependence of sheet resistance on the ion energy. (a) As ion implantation, (b) BF_2 ion implantation

RTA is essential for 10-keV BF_2 implantation to obtain low

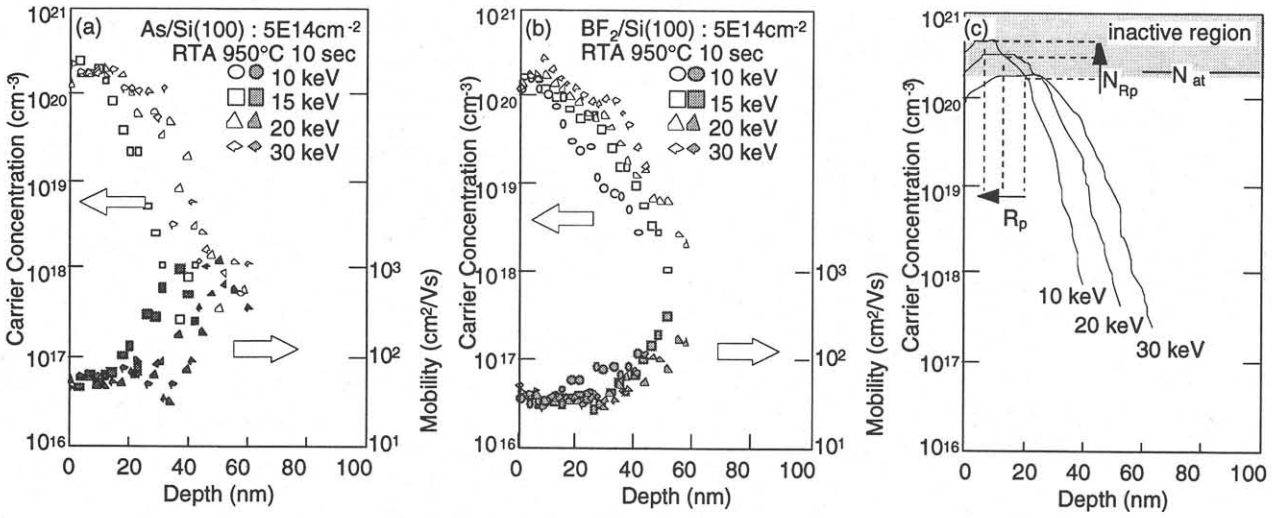

Fig. 3 Depth profiles of carriers and mobility.
(a) As ion implantation, (b) BF_2 ion implantation,
(c) Model of energy dependence of carrier activation

sheet resistance (Fig. 2), because the recrystallization seemed to be imperfect when FA was used. In the case of 30-keV BF_2 implantation, impurities were fully activated after RTA. On the other hand, the activation ratio was only 40% with the 10 keV implantation of both BF_2 and As.

To clarify the cause of the lower activation in the case of 10-keV implantation, carrier profiles were obtained by stripping Hall measurement. Figure 3 shows the carrier and mobility profiles of the As or BF_2 implanted samples at a dose of 5 X 10^{14} cm^{-2} after RTA. The junction depth (x_j) became shallower as the ion energy decreased. When the ion energy is decreased, the projection range (R_p) is expected to be closer to the surface and the peak carrier concentration (N_{Rp}) becomes higher as illustrated in Fig. 3(c). However, the peak carrier concentration is observed to be almost the same at about 2 x 10^{20} cm^{-3} for BF_2 and 3 X 10^{20} cm^{-3} for As. This is because the implanted impurities at concentrations these levels are not activated.

Thus, the implantation dose must be optimized to obtain ultra-shallow diffused layers with low resistance. A dose above 3 X 10^{14} cm^{-2} is essential when the ion energy is lowered to less than 10 keV, and with a dose of 5 X 10^{14} cm^{-2}, we have obtained sufficiently low sheet resistance of 0.7 kΩ/sq. for BF_2 and 0.4 kΩ/sq. for As.

III. n-MOSFET Fabrication Process

To suppress the short-channel effect and to reduce V_{th} for low-power operation, B ions were implanted as a punchthrough stopper, and As ions as counter-doping. Then ,a 4-nm-thick gate oxide and a P-doped poly-Si gate were formed. E-beam lithography was used to fabricate the gate electrode. After gate formation, low-energy As implantation was performed. This was followed by deep As ion implantation, then RTA was used to activate implanted impurity.

IV. Parasitic Resistance of 0.15-μm n-MOSFETs

We used the Chern method[3] to estimate the total S/D parasitic resistance of the n-MOSFETs. The fabricated devices are listed in Table 1. The S/D ultra-shallow diffused layers were formed by As implantation with an ion energy ranging from 10 to 20 keV (implanted doses either 1 X 10^{14} or

Table 1 Fabricated n-MOSFET samples

No.	implantation.	RTA	Rsd(Ω)	ρs(Ω/sq.)	plot
#1	10 keV, 1E14 cm-2	950°C 10 s	106.9	1.27 k	none
#2	10 keV, 5E14 cm-2	950°C 10 s	59.6	0.34 k	▲
#3	15 keV, 1E14 cm-2	950°C 10 s	78.4	0.84 k	none
#4	15 keV, 5E14 cm-2	950°C 10 s	53.0	0.29 k	□
#5	20 keV, 1E14 cm-2	950°C 10 s	61.8	0.56 k	none
#6	20 keV, 5E14 cm-2	950°C 10 s	40.2	0.25 k	○

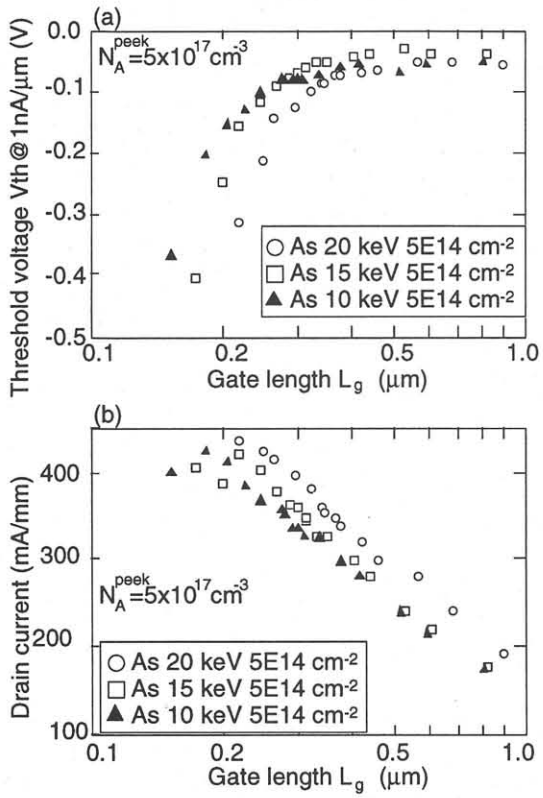

Fig. 4 Gate length (L_g) dependence of n-MOSFET characteristics (a)V_{th} vs L_g, (b)I_d vs L_g

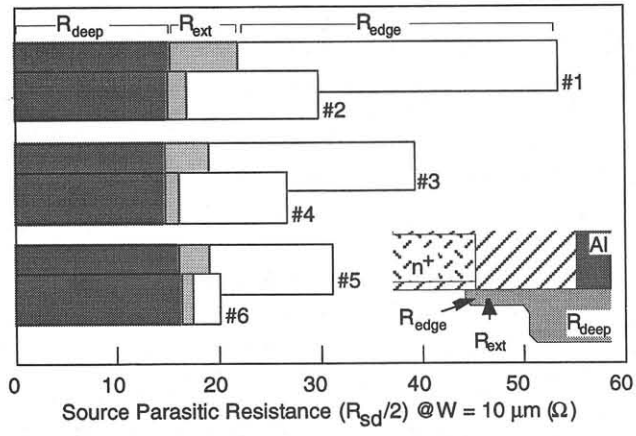

Fig. 5 Sourceparasitic resistance (R_{sd}/2) as a function of ion energy. RTA was carried out at 950°C for 10 s.

5 X 10^{14} cm^{-2}). The dependence of threshold voltage (V_{th}) and drain current (I_d) on the gate length (L_g) are shown in Fig. 4. The n-MOSFET fabricated using 10 keV As implantation shows better short-channel characteristics due to its shallower junction. However, it has a lower I_d. The S/D parasitic resistance (R_{sd}) is also shown in Table 1. The R_{sd} consists of the resistance of the ultra-shallow diffused layer (R_{ext}), the deep-diffused layer including the contact resistance (R_{deep}), and the edge resistance due to current crowding[4] (R_{edge}). As the ion energy was decreased, source resistance (= R_{sd}/2) increased as shown in Fig. 5, and this increase was larger when the implanted dose was 1 x 10^{14} cm^{-2}. Since R_{deep} and the sheet resistance of the shallow diffused layer are almost constant, this increase is due to the increased S/D edge resistance. This observation contradicts the prediction that a shallow, abrupt diffused layer has smaller edge resistance[4]. Therefore, knowledge about two-dimensional dopant profiles is becoming more and more important in the fabrication of high-performance MOSFETs with gate length of less than 0.15 μm.

VI. Conclusion

In low-energy ion implantation for S/D formation in 0.15-μm MOSFETs, degradation of the carrier activation and an increase in S/D edge resistance were found for the first time. These phenomena should be considered when using low-energy ion implantation to fabricate high-performance 0.15-μm MOSFETs.

Acknowledgments

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