# A Novel Functional Logic Gate Using Resonant-Tunneling Devices for Multiple-Valued Logic Applications 

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#### Abstract

We have proposed a novel functional logic circuit, or an analog-to-quaternary quantizer. The logic function is based on the monostable-multistable transition in a circuit consisting of series-connected resonant-tunneling devices. By using the integration technology of InGaAs-based resonant-tunneling diode (RTD) and HEMT, we fabricated the circuit and obtained the successful room-temperature operation. As a result, the operation principle is confirmed. Consisting of six RTDs and one HEMT, the circuit is much simpler than conventional ones.


## 1. Introduction

The negative differential resistance (NDR) of resonant tunneling (RT) devices allows us to implement functional circuits with reduced complexity. In particular, by connecting RT devices in series, we obtain a multiple-peak structure in the current-voltage characteristics, which provides RT devices with a great advantage over conventional ones in the field of multiple-valued logic (MVL) applications. The MVL circuits with RT devices proposed so far, however, still have limited functions.

To further the capability of RT devices in MVL applications, we have proposed a new class of MVL circuits that exploits a unique aspect of series-connected RT devices: monostable-multistable transition logic (MML). ${ }^{1)}$ Logic
operation is performed by the selection of one stable point from others during the transition. This selection is possible through the modulation of the peak current by input signal.

In this paper, after reviewing the basic idea of MML, we propose a novel analog-to-quaternary quantizer based on the MML concept. We then describe InGaAs-based RTD/HEMT integrated devices that were used to implement the circuit. Finally, experimental results on the successful room-temperature operation are presented. The circuit, consisting of six RTDs and one HEMT, is much simpler than conventional MVL circuits.

## 2. Basic Idea of MML

The operation of MML is explained as follows. Consider a circuit consisting of series-connected resonant-tunneling


Fig. 1 A monostable-multistable transition logic (MML) circuit with resonant-tunneling transistors ( $\mathrm{RTT}_{1}$ to $\mathrm{RTT}_{\mathrm{N}}$ ) (a), schematics showing the transition from a monostable state (b) to a multistable state (c), and an MML operation (d). In (c), one stable point $(\bigcirc)$ is selected among others $(\bigcirc)$ when $\mathrm{V}_{\mathrm{CLOCK}}$ changes from $\mathrm{V}_{1}$ to $\mathrm{V}_{2}$, because peak currents $\mathrm{P}_{\mathrm{M}+1}$ and $\mathrm{P}_{\mathrm{M}+2}$ are larger than $\mathrm{P}_{1}$ but smaller than $\mathrm{P}_{2}$.

[^0]transistors. These transistors are assumed to have negative differential output resistance and their peak current can be modified by the gate voltage. These devices have been fabricated in several manners, ${ }^{2-4)}$ and we denote them as RTTn ( $\mathrm{n}=1$ to N ) in Fig. 1(a). When the supply voltage $\mathrm{V}_{\text {CLOCK }}$ increases from low $\left(=\mathrm{V}_{1}\right)$ to high $\left(=\mathrm{V}_{2}\right)$, the circuit state evolves from a monostable state (Fig. 1(b)), where all the RTTs remain in the low output-resistance branch (onstate), into a multistable state (Fig. 1(c)), where some RTTs switch from the low-resistance branch (on-state) to the highresistance one (off-state). During this monostablemultistable transition, the switching sequence of the RTTs is dominated by a simple law: the smaller its peak current, the earlier it switches. Therefore, if the input signal can modify the peak current, it can control the switching sequence and thus determine the RTTs that switch at $\mathrm{V}_{\text {CLOCK }}=\mathrm{V}_{2}$. As a result, the output voltage $\mathrm{V}_{\text {OUT }}$ is obtained at $\mathrm{V}_{\text {CLOCK }}=\mathrm{V}_{2}$ in accordance with the input signal (Fig. 1(d)). The output is multiple-valued, because it is proportional to the number of the switched RTTs that are placed between the output terminal and the ground.

## 3. Device Structure

To fabricate MML circuits, it is necessary to obtain the RT device, the peak current of which can be modulated by the gate voltage. For this purpose, an integrated device consisting of an InGaAs-based RTD and a HEMT connected in parallel is applicable (Fig. 2). ${ }^{4}$ ) Since the total current flowing through this integrated device is the sum of the RTD current and the HEMT drain current, the peak current of the device can be modulated by the HEMT gate voltage. This characteristics satisfy the requirement for the RTT described above. For the quantizer discussed below, we used an integrated device made of a parallel connection of three series-connected RTDs and one HEMT as shown in Fig. 3.

As for the heterostructure of the HEMT, we grew a 200nm ud-InAlAs buffer layer, a $15-\mathrm{nm}$ ud-InGaAs channel layer, a 2-nm ud-InAlAs spacer layer, a $4-n m n^{+}-I n A l A s ~(1 \times$ $10^{19} \mathrm{~cm}^{-3}$ ) carrier supply layer, a $20-\mathrm{nm}$ ud-InAlAs layer, and an $\mathrm{n}^{+}-\operatorname{InAlAs}(15 \mathrm{~nm}) / \operatorname{InGaAs}(20 \mathrm{~nm})\left(1 \times 10^{19} \mathrm{~cm}^{-3}\right)$ cap layer on a semi-insulating InP substrate in this order by MBE. For the RTD, a $150-\mathrm{nm}$ n-InGaAs $\left(1 \times 10^{18} \mathrm{~cm}^{-3}\right)$ collector layer, a $1.5-\mathrm{nm}$ ud-InGaAs spacer layer, a doublebarrier structure of ud- $\mathrm{In}_{0.53} \mathrm{Ga}_{0.47} \mathrm{As}(1.2 \mathrm{~nm}) / \mathrm{ud}-\mathrm{InAs}(2.8$ $\mathrm{nm}) / \mathrm{ud}-\mathrm{In}_{0.53} \mathrm{Ga}_{0.47} \mathrm{As}(1.2 \mathrm{~nm})$ sandwitched by $1.4-\mathrm{nm}$ udAlAs barriers, a $1.5-\mathrm{nm}$ ud-InGaAs, and a $100-\mathrm{nm} \mathrm{n}-\mathrm{InGaAs}$ $\left(1 \times 10^{18} \mathrm{~cm}^{-3}\right)$ emitter layer, and finally an $\mathrm{n}^{+}$-InGaAs $(2 \times$ $10^{19} \mathrm{~cm}^{-3}$ ) cap layer were grown also by MBE on top of the HEMT structure. Conventional wet-etching technique and metal deposition followed by lift-off process were used in the device fabrication. Details were described in Ref. 4. The transconductance of a $0.7-\mu \mathrm{m}$ gate HEMT was $600 \mathrm{mS} / \mathrm{mm}$, while the RTD peak current density was $9 \times 10^{4} \mathrm{~A} / \mathrm{cm}^{2}$.

## 4. Circuit Implementation

We implemented an MML analog-to-quaternary quantizer by using six RTDs connected in series with one


Fig. 2 A resonant-tunneling transistor (RTT) and an RTD and a HEMT connected in parallel (a) and an integrated device structure (b). The peak current of this integrated device can be modulated by the HEMT gate voltage through the variation in the drain current.


Fig. 3 An MML analog-to-quaternary quantizer fabricated in this study (right). The RTD peak current ratio is $\mathrm{A}: \mathrm{B}: \mathrm{C}: \mathrm{X}: \mathrm{Y}: \mathrm{Z}=2: 1.8: 1.6: 1.4: 1.2: 1$. The circuit representation used in Fig. 1(a) is also shown (left).


Fig. 4 Peak currents (diamonds, squares and triangles) in $\mathrm{I}-\mathrm{V}$ characteristics between the $\mathrm{V}_{\text {OUT }}$ terminal and the ground in Fig. 3 as a function of the input voltage $\mathrm{V}_{\mathrm{IN}}$. Peak currents of $\mathrm{A}, \mathrm{B}$, and C are also shown by the dashed lines. The three peak currents are lower than those of $\mathrm{A}, \mathrm{B}$ and C for $\mathrm{V}_{\text {IN }}<0.05 \mathrm{~V}$, while they are larger for $\mathrm{V}_{\mathrm{IN}}>0.45 \mathrm{~V}$.

HEMT as shown in Fig. 3. As the input signal $\mathrm{V}_{\text {IN }}$ increased, the peak currents of the RTD-HEMT integrated device increased. To obtain the quatizer function, the ratio of the RTD areas was designed so that all of the RTD-HEMT peak currents were smaller than those of the RTDs, A, B and C, for a small input $\left(\mathrm{V}_{\mathrm{IN}}<\mathrm{V}_{\text {th }}\right)$, while they were larger for a large input $\left(\mathrm{V}_{\text {IN }}>\mathrm{V}_{\mathrm{th} 3}\right)$. This requirement was satisfied by setting the RTD area ratio such that $\mathrm{A}: \mathrm{B}: \mathrm{C}: \mathrm{X}: \mathrm{Y}: \mathrm{Z}=$ 2:1.8:1.6:1.4:1.2:1. Figure 4 shows that if $\mathrm{V}_{\mathrm{IN}}<0.05 \mathrm{~V}$ (= $\mathrm{V}_{\text {th1 }}$ ), all of the RTD-HEMT peak currents are smaller than those of $\mathrm{A}, \mathrm{B}$, and C . In this case, when $\mathrm{V}_{\text {Clock }}$ increases from 0 V to 3.2 V (this value is selected to be large enough but not too large for three RTDs out of the six to switch off), the three RTDs, X, Y, and Z, switch from on to off and then $\mathrm{V}_{\text {OUT }}$ is expected to be the highest. If $0.05 \mathrm{~V}<\mathrm{V}_{\text {IN }}<0.25 \mathrm{~V}$, two of the RTD-HEMT peak currents are smaller than that of C, and, therefore, the RTDs, $\mathrm{Y}, \mathrm{Z}$ and C , switch off. The output is thus the second highest. Similarly, for $0.25 \mathrm{~V}<\mathrm{V}_{\text {IN }}$ $<0.45 \mathrm{~V}$ and $0.45 \mathrm{~V}\left(=\mathrm{V}_{\mathrm{th} 3}\right)<\mathrm{V}_{\text {IN }}$, the outputs are expected to be the third highest and the lowest, respectively.

Figure 5 shows the experimental result of the circuit operation. The quaternary output was obtained with the threshold voltages of $0.05,0.25$ and 0.40 V . These values agree well with the predicted ones described above. We also succeeded in fabricating analog-to-ternary quantizers with four RTDs and a HEMT. These quantizers are valuable for obtaining the complement function in MVL and for digitizing an analog signal into multiple-valued data.

It should be noted that the MML quaternary quantizer is compact compared with conventional circuits. For example, 31 transistors with three different threshold voltages are necessary if the voltage-mode CMOS circuit is used. ${ }^{5)}$ Because of this reduction in circuit complexity, high-speed operation is expected for the quantizer presented here.

## 5. Conclusions

We proposed an MML analog-to-quaternary quantizer. By using the InGaAs-based RTD/HEMT integration technology, we fabricated the circuit and obtained the


Fig. 5 Analog-to-quaternary quantizer operation obtained at room temperature. As input voltage $V_{\text {IN }}$ increases from -0.1 V to 0.5 V in $0.05-\mathrm{V}$ steps, $\mathrm{V}_{\text {out }}$ is quantized into quaternary values, $2.8,2.2$, 1.5 , and 1.2 V .
successful room-temperature operation. As a result, the operation principle was confirmed. Consisting of six RTDs with one HEMT, the circuit is much simpler than conventional MVL circuits.

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