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Lithographic Technologies for 1-Gb DRAMs and Beyond

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1. Introduction

The development of ultra-large-scale integrated circuits (ULSIs) over the last 15 years has been dramatic. The bit capacity of memory devices has quadrupled every two-three years due to new developments in microfabrication technologies. All of these developments have been attained by using optical lithography. However, the minimum feature size of the most advanced memory devices has almost reached the wavelength of the exposure light.

High pressure mercury lamps have generally been used as the light source of the optical stepper. [1] The need for further miniaturization is forcing the introduction of much shorter wavelength light, such as KrF excimer laser light (248 nm). The strong demand for larger memory capacity has put the use of lithographic technology for memory devices at the forefront of the miniaturization of semiconductor devices. The recent demands for higher speed logic circuits have now led to the need for logic devices with very fine pattern delineation.

Figure 1 shows the trend towards miniaturization of ULSI devices. As shown in this figure, several lithographic technologies will be applicable to 1-Gb DRAM fabrication from the viewpoint of resolution. However, there are many other factors to be considered. In this paper, the critical lithographic issues for the delineation of 1-Gb DRAM patterns will be discussed.

2. Chip-Size Estimation

Assuming a conventional stacked capacitor cell (STC), the area of a memory cell is

$$Acell = (4F+3X)(2F+2X), \quad \text{----- (1)}$$

where F is the minimum feature size and X is the overlay tolerance.[2]

As shown in this expression, not only the minimum feature size but also the overlay tolerance contributes significantly to determining the cell area. The overlay tolerance has been 20% to 30% of the minimum feature size. Figure 2 shows the memory cell size dependence on the overlay tolerance. If we assume the overlay tolerance as 25% of the minimum feature size, memory cell size Acell is about 12 times the square of the minimum feature size, F. Namely, Acell is $12F^2$. We call this coefficient the memory cell coefficient. In the case of fully self-aligned structure, X in the expression (1) can be neglected. Then Acell becomes $8F^2$.

The chip sizes of the memory devices can be calculated from the cell area, defining the ratio of the memory cell area to the total chip area as Rcc. In the conventional DRAM devices, Rcc is usually around 50% to 60% depending on the design of the peripheral circuits. Using these parameters, the memory chip area can be obtained using

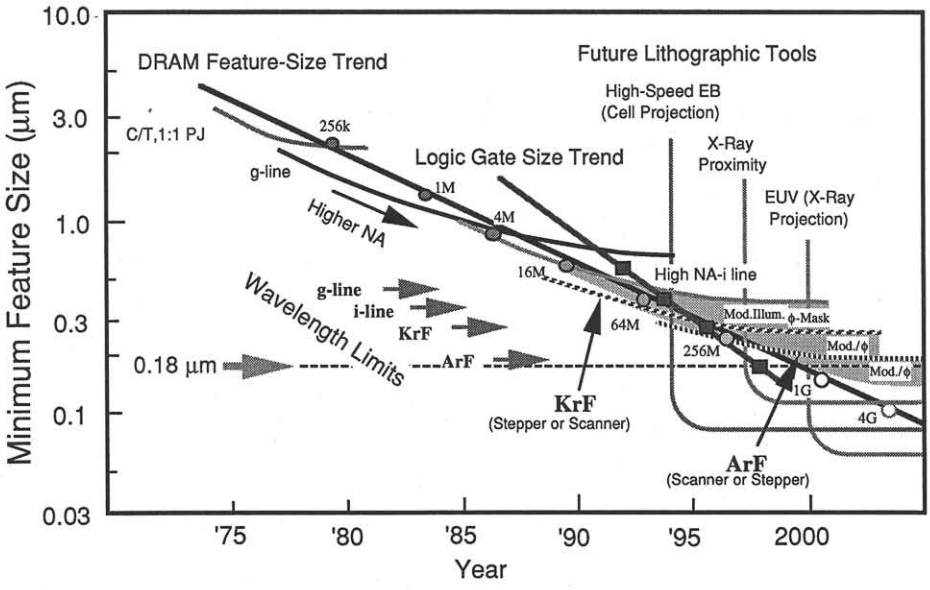

Figure 1. Miniaturization trend in DRAMs and logic devices and evolution of lithography technologies

$$Achip = M \times Acell/Rcc, \text{-------- (2)}$$

where M is the bit capacity of the memory devices.

Using this expression, the size of various type chips can be calculated, as shown in Fig. 3. We assume that if more than 50 chips can be obtained from 8"Φ wafers and 100 chips from 12"Φ wafers, they will be worth sampling; if more than 100 chips are obtained from 8"Φ wafers and 200 chips from 12"Φ wafers, they will be profit-making.

From this figure, it can be seen that if the minimum feature size is larger than 0.13 μm, the chip size will not be a profit-making size, even if the memory cell coefficient is $8F^2$ (fully self-aligned structure) and 60% Rcc. There are several proposals for a $6F^2$ cell structure.[3,4] If we can achieve this cell structure, chip size will be in the profit-making area with a minimum feature size of 0.15 μm. Such improvements in the device structure will relax the requirements on micro-fabrication technology, and thus help compensate for delays in the development of micro-fabrication technology.

3. Resolution in Optical Lithography

Obtaining high resolution with a certain depth of focus (DOF) is the most critical issue in optical lithography. The resolution of optical lithography is governed by the well-known Rayleigh equation. Figure 4 shows the relationships between the exposure-light wavelength and resolution of several optical lithography techniques. The width of the V-shaped patterns indicates process and/or design latitude. As shown in the figure, using the same wavelength light and the same type of resolution-enhancement technology, higher resolution always gives smaller process and/or design latitude. Planarization will thus be indispensable for the continuing use of optical lithography.

4. Other Issues for Future Lithography

Thinner resists will be required for relaxing the required depth of focus in optical lithography. Not only the DOF problem, but also the aspect ratio of the resist pattern, will be key issues in all lithographic technologies. A higher resolution will increase the aspect ratio of the resist pattern. However, high-aspect ratio conditions lead to patten collapse.[5] Thinnner resists will help prevent pattern collapse in optical lithography and in other lithographies. The biggest obstacle to using thinner resists is the need for high dry eching selectivity.

Critical dimension(CD) control will become an important issue as the need to reduce CD variation becomes stronger and stronger. Recent logic devices require less than 10% gate length variation in 0.2 μm and smaller patterns. This means the pattern deviation must be controlled to 20 nm or less. Not only pattern size control, but also measurement of the pattern itself, is very difficult. New mesurement systems are thus needed.

In optical lithography, defocusing and light reflection are the main causes of CD variation. Chemically amplified resists will be commonly used in future lithographies, and acid diffusion is a big factor in CD control for this type of resist system.[6] Mask-size control is a critical issue in CD control for optical and X-ray lithography.

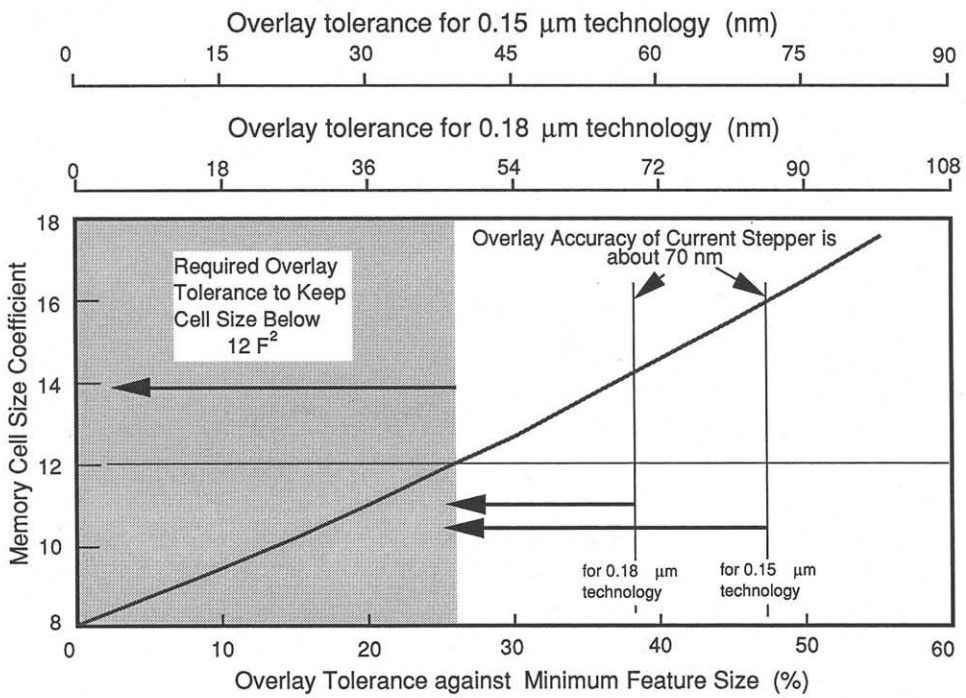

Figure 2. Relationship between overlay tolerance and memory cell size.

5. Conclusion

A 0.18 μm minimum feature size is not small enough for obtaining profit-making memory chips. Patterns 0.13 μm or smaller are required without adopting a new memory cell structure. In any of the lithographic technologies, obtaining such fine pattern sizes requires making the resist very thin in order to make the aspect ratio small; tighter overlay tolerances are indispensable for making smaller cells. Total planarization makes it possible to use thinner resists, and the self-aligned technique makes it possible to ease the effective overlay tolerance. However, simply introducing these new technologies is not sufficient. The total process (lithography, dry etching, film deposition, planarization, etc.) must be optimized and a smart-device structure must be introduced. Without such optimization and improvements in device design, a practical, profit-making Giga-bit technology will not be attained.

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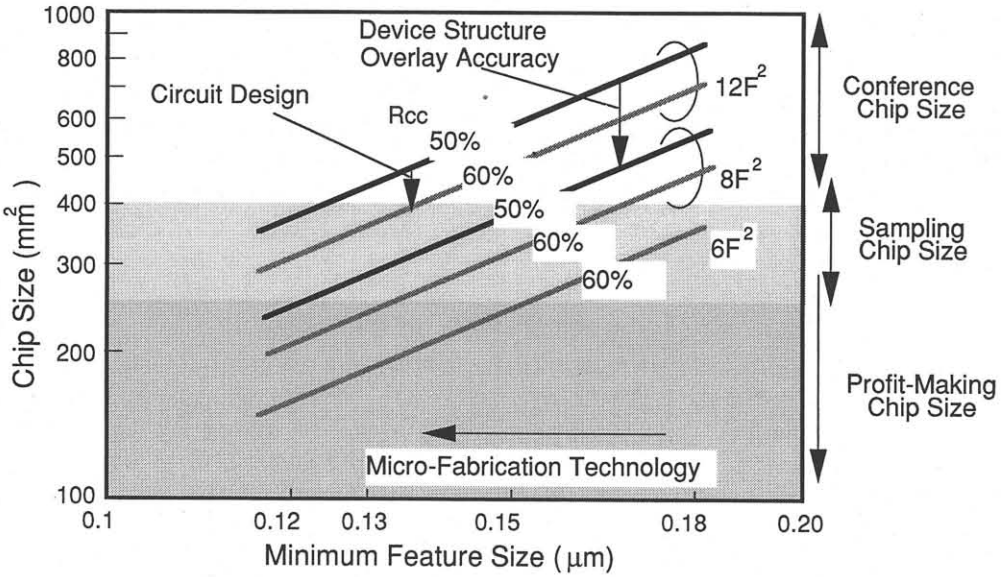

Figure 3. Relationship between minimum feature size and chip size.

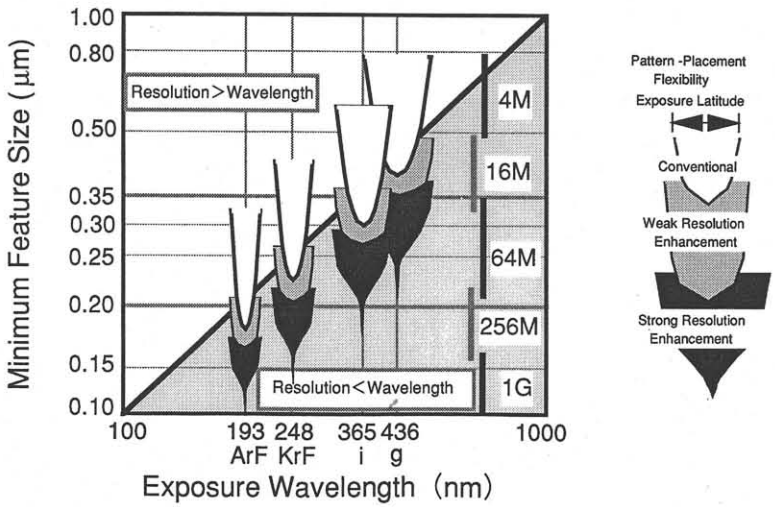

Figure 4. Optical lithography roadmap.